Lab Manual for Communication Lab

Ministry of Higher Education
Mansoura Higher
Institute of Eng .& Tech.
Communications and Electronics Department

وزارة التعليم العالي
معهد المنصورة العالي للهندسة والتكنولوجيا
قسم هندسة الاتصالات والإلكترونيات

Digital Communication Lab Manual

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Analog to Digital Converter

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Curriculum Objectives

1. To understand the operation theory of analog to digitalconverter.
2. To understand the operation theory and characteristics ofADC0804 and ADC0809.
3. To implement the analog to digital converter by usingADC0804 and ADC0809.

Curriculum Theory

In general, the continuous signal that we measure in voltage or current status is called as analog signal. If via a device that can convert the analog signal to digital signal, then we called this device as analog to digital converter (ADC). ADC can reduce the effect of noise and by using the technique of coding, ADC has the function of debugging. On the other hand, digital signal can also be easily stored. Next we will discuss on the basic theory of the analog to digital converter.

1. The Operation Theory of ADC

Figure 7-1 is the characteristic curve of an ideal 3-bit analog to digital converter, and the analog input range is from 0 V to 1 V. We can divide the input signal into 8 ranges, at each range all the analog values use the same binary code to represent, and this binary code is corresponding with the mid-value. Therefore, during the processing of converter, it consists of ± 1/ 2 least significant bit (LSB) quantization uncertainty or quantization error, and also includes the previous converter that has the analog error, then all of the errors comprise the error value of ADC. One of the methods to reduce the quantization error is to increase the number of bits of the converter.

Quantization value (Q) means when the digital output changes 1 LSB, the required input voltage value also changes, the expression is

$$Q = \frac{FS}{2^n - 1} = \frac{1}{2^n} \quad (7\text{-}1)$$

Where FS is the full scale, the value equals to $[(2^n - 1) / 2^n]$, 2^n is defined as resolution, where n is the ADC digital output bit, so when the larger the value of n, the higher the resolution. In general, the ADC technical manual defmes resolution in bits. For example, the resolution of ADC0804 is 8 bits.

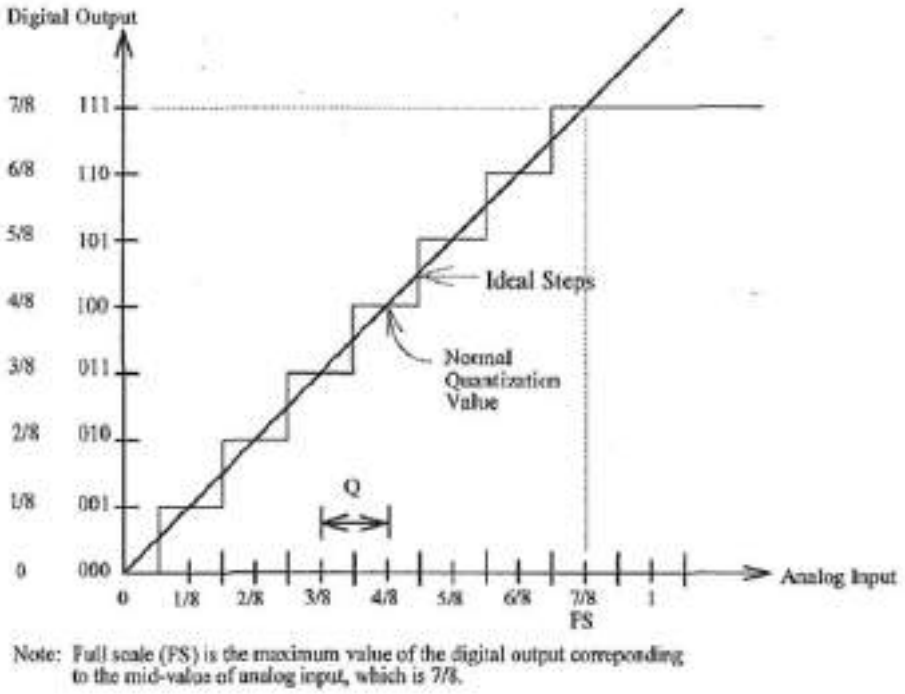


Figure 7-1 The ideal waveform of analog to digital converter.

The methods of conversion for analog to digital converter are various, normally can be divided as .A/D conversion methods are digital-ramp ADC, successive approximation ADC, flash ADC and tracking ADC. In this chapter, only the successive approximation ADC is discussed, therefore, we will discuss on the o

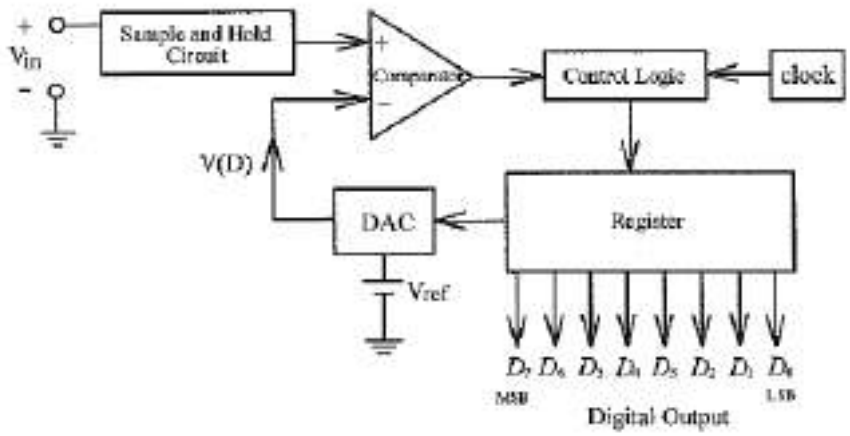


Figure 7-2

The basic block diagram of successive approximation ADC.

Figure 7-2 is the block diagram of successive approximation ADC, which is provided with 8-bit resolution. When we input the analog signal, sample-and-hold, S&H circuit will capture the input signal V_{in} to avoid any signal change during conversion period. At this moment, the control logic will store all the bits and reset to "0", follow by the most significant bit, MSB D_7 is set to "1". Thus, the output voltage of DAC is

$$V(D) = 2^{n-1} \times Q = 2^{n-1} \times \frac{V_{ref}}{2^n} = \frac{1}{2} V_{ref} \qquad (7\text{-}2)$$

This voltage is half of the reference voltage V_{ref} • If the input voltage V_{in} is higher than V(D), then D_7 remains at" 1 ", otherwise alters to " 0 ". Next, make second bit D_6 as " 1 ", after passing through a DAC then obtainan output voltage V(D), at this moment comparing the new V(D) and V_{in}, ***if*** V_{in} is higher than V(D), then D_6 remains at " 1 " otherwise alters to " 0 ". Similarly for the others until the comparison of D_7 to D_0 have been completed, then we can obtain the complete D_7 to D_0 digital output.

2. ADC0804 Analog to Digital Converter

ADC0804 is a 20-pin DIP package with an 8-bit resolution single channel IC. The analog input voltage range is from 0 V to 5 V with single 5 V power supply, 15 mW power consumption and 100 µs conversion time. As a result of this IC contains of 8-bit resolution, so it has $2^8 = 256$ quantization steps, if the reference voltage is 5 V, each step will be 5/256 = 0.01953 V. 00000000 (00H) represents 0.00 V and 1111111 (FFH) represents 4.9805 V. The unadjusted error of ADC0804 is ±1 LSB, which is 0.01953 V, which includes full-scale error, offset error and non-linearity error.

Figure 7-3 shows the pins diagram of ADC0804. In figure 7-3, the Do to D_7 of ADC0804 is the 8-bit output pins, when CS and RD are low, the digital data will be sent to the output pins. If any pins of CS and RD are high, then D_0 to D_7 are in floating condition.

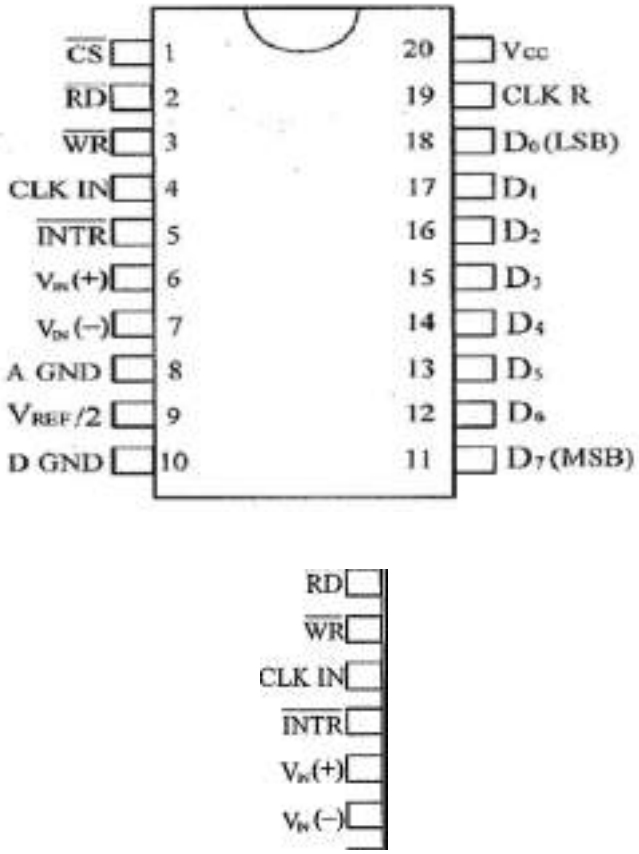


Figure 7-3 The pins diagram of ADC0804.

$\overline{WR}$; is the write control signal, when $\overline{cs}$ and $\overline{WR}$ are Low, ADC0804 will do the clear action, when $\overline{WR}$ backs to high, ADC will start the conversion. CLK IN (Pin 4) is the clock input, the frequency range starts from 100 kHz to 800 kHz. During the conversion period, $\overline{INTR}$ is at high level and then after the conversion completed, $\overline{INTR}$ will alter to low. Pin 6 $V_{in}(+)$ and pin 7 $V_{in}(-)$ are differential analog signal inputs, ordinarily used single input terminal and $V_{in}(-)$ is connected to ground. ADC0804 has two ground terminals, one is analog ground (A GND) and another one is digital ground (D GND). Pin 9 $(V_{ref}/2)$ is 1/2 of the reference voltage, if pin 9 is floating, then the 1/2 reference voltage equals to power supply voltage V_{cc} ADC0804 has a built-in Schmitt trigger as shown in figure 7-4. If we add a resistor and capacitor at CLK R (pin 19) and CLK IN (pin 4), then we can generate the ADC operating time, where the frequency is

$$f_{CLK} \approx \frac{1}{1.1 \times RC} \ (Hz) \qquad (7\text{-}3)$$

Therefore, we need not input an external clock signal to CLK IN terminal. We can determine the clock signal by the external R and C via pin 4 and pin 19.

Figure 7-5 is the circuit diagram of ADC0804 analog to digital converter, the analog signal input range is controlled by VR_2 and input through the $V_{in}(+)$ terminal and at the same time, the $V_{in}(-)$ is short

circuit. $V_{ref}/2$ is provided by R_1, R_2 and VR_1. C_1 and R_3 is used to control

the clock of the circuit, $\overline{CS}$ and $\overline{RD}$ are short circuit, so that the IC is enable, then let $\overline{WR}$ and $\overline{INTR}$ connect to SW_1 in order to simulate the control signal.

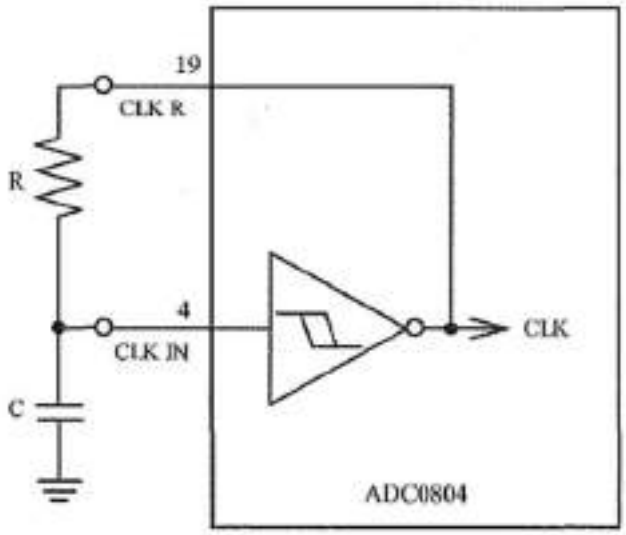


Figure 7-4 The internal circuit diagram of ADC0804.

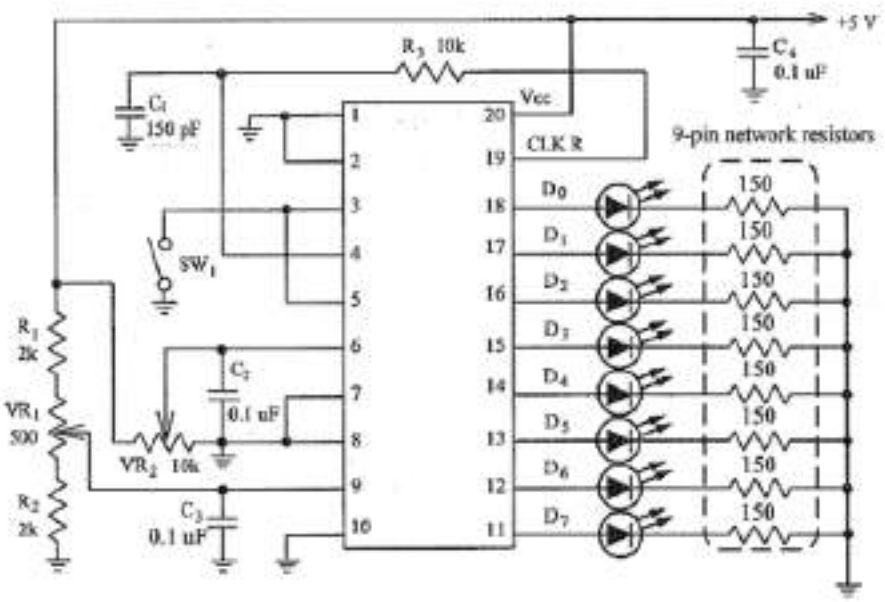


Figure 7-5 The circuit diagram of ADC0804 circuit.

3. ADC0809 Analog to Digital Converter

ADC0809 is a 28-pin DIP package, which has 8-bit resolution and 8-channel multiplexer IC. It operates with 5 V single power supply, the input analog voltage range is from 0 V to 5 V and the power consumption is 15 mW. The 8-channel multiplexer can directly access any of 8 single-ended analog signals. With 8-bit resolution, the ADC0809 have 2^8 = 256 quantization steps. Therefore, for the 5 V voltage power supply condition, each step is 5 V /256, so the quantization value (Q) is 0.01953 V. So 00000000 (00H) represents 0.00 V and 11111111 (FFH) represents (255 / 256) x 5 = 4.9805 V . The unadjusted error is ±1 LSB, which is same as 0.01953 V where it contains of full-scale error, offset error, non-linearity error and multiplexer error. ADC0809 needs a group of clock input signals to operate, the frequency range of the clock signal starts from 10 kHz to 1280 kHz. At 640 kHz clock frequency, the typical conversion time is 100 µs.

Figure 7-6 is the pins diagram of ADC0809. In figure 7-6, the ADC0809pins 5, 4, 3, 2, 1, 28, 27 and 26 are the 8 input ports, which is IN_7 to IN_0 Pins 21, 20, 19, 18, 8, 15, 14 and 17 are the output ports, which are D_7 to D_0 and pin 10 is the clock input port. Pin 11 is the power supply V input port and pin 12 is the positive reference voltage $V_{ref}(+)$ input port. Normally, pins 11 and 12 are connected together. Pin 13 is grounded and pin 16 is the negative reference voltage $V_{ref}(-)$ input port that normally connects to ground pin 13. The selections of channels are controlled by pins 25, 24 and 23 which are ADD A, ADD B and ADD C. If select pin 26 (IN_0) as input port, then connect 23, 24 and 25 to ground.

ADC0809 can be easily connected with microprocessor, where pin 6 (START), pin 7 (end of conversion, EOC), pin 9 (output enable, OE) and pin 22 (address latch enable, ALE) are normally used to control the ADC and the clock of data conversion of microprocessor. When ADC0809 conversion is finished, EOC can enable the central processing unit (CPU). When CPU is ready to receive data, it will enable pin OE and read the data. After that enables ALE and START, to let ADC0809 continue the next conversion. If under the condition of using

multi-channel inputs, pins 23 (ADD C), 24 (ADD B) and 25 (ADD A), ALE and START must be set during the period of enable.

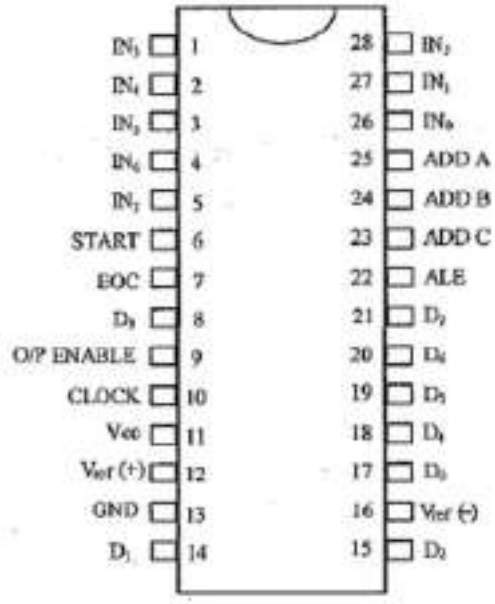


Figure 7-6 The pins diagram of ADC0809.

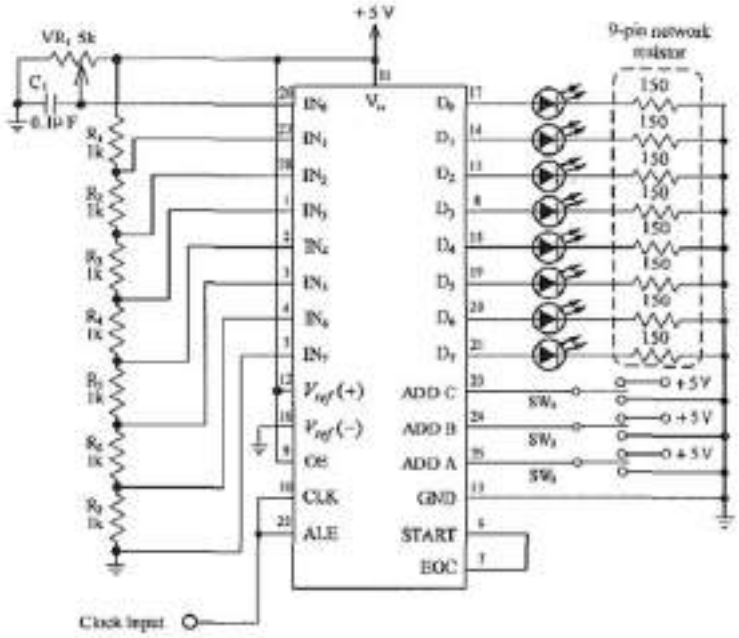


Figure 7-7 The circuit diagram of ADC0809.

Figure 7-7 is the circuit diagram of ADC0809 analog to digital converter, which EOC (pin 7) output signal is the START input signal, and the ALE and CLK output signal are the clock signal. The input signal rangeof analog input port IN_0 is determined by VR_1. The IN_1 to IN_7 input signal ranges are determined by R_1 to R_7, which is a group of resistor networks. The channel selection is controlled by SW_1, SW_2 and SW_3. We use LED to represent the digital output, therefore, LED "on" represents "1" and LED "off' represents "0". The brightness of the LED depends on the current of flowing through, so it is related to the serial resistors pack.

Experiment 1: ADC0804 analog to digital converter

1. Refer to figure 7-5 or ETEK DA-2000-04 module, let JI open circuit.
2. Adjust VR_1 and use the digital voltage meter to measure the voltage of Vref / 2 input terminal (pin 9), then adjust VR_1 until Vref / 2 input terminal voltage is 2.5 V. At this moment, ADC0804 analog voltage input range starts 0 V to 5 V.
3. Adjust VR_2 so that the input voltage of the analog signal input terminal (which is pin 6) is 0 V.
4. Let JI short circuit and connect to ground, then maintain the output digital signal. Observe on the change of LED, LED "on" represents "l", LED "off' represents "0", finally record the measured results in table 7-1.
5. Let JI open circuit, the digital output will be varied from the analog input signal.
6. Adjust VR_2, so that the input voltage of the analog signal input terminal is similar to the values in table 7-1, then repeat step 4 and step 5.

Experiment 2: ADC0809 analog to digital converter

1. Refer to figure 7-7 or ETEK DA-2000-04 module.
2. From CLK input terminal, input a 120 kHz frequency, 2 V_{pp} amplitude, and a square wave with 1 V_{pp} offset (i.e. high is 2 V, low is 0 V).
3. Let SW3, SW2 and SW_1 switch to GND (push down the slide switch), at this moment, the analog signal is inputted from the IN_0 input.
4. Adjust VR_1 so that the input voltage of the analog signal input terminal IN_0 is similar to the values in table 7-2.
5. Observe on the changes of LED, LED "on" represents "l", LED "off' represents "0", then record the measured results in table 7-2.
6. Calculate the output voltage of the input terminal IN_1 to IN_7, then record the measured results in table 7-3.
7. Refer to table 7-3, by using SW_3, SW_2 and SW_1, select the different input terminals (IN1 to IN_7) as the analog input.
8. Observe on the changes of LED, then record the measured results intable 7-3

Table 7-1 The measured results ofADC0804.

Analog Input Voltages (V)	Digital Output	
	Ideal Values	Experiment Values
	Binary Digits	Binary Digits
0.0		
0.5		
1.0		
1.5		
2.0		
2.5		
3.0		
3.5		
4.0		
4.5		
5.0		

Table 7-2 The measured results of ADC0809 single channel input.

Analog Input Voltages (V)	Digital Output	
	Ideal Values	Experiment Values
	Binary Digits	Binary Digits
0.0		
0.5	-	
1.0		
1.5		
2.0		
2.5		
3.0		
3.5		
4.0		
4.5		
5.0		

Table 7-3 The measured results of ADC0809 multi-channel input.

SW_3	SW_2	SW_1	Analog Input(Ideal Value)		Digital Output (Experiment Value)
			Input Terminal	Voltage(V)	Binary Digits
GND	GND	+5V	IN_1		
GND	+5V	GND	IN_2		
GND	+5V	+5V	IN_3		
+5V	GND	GND	IN_4		
+5V	GND	+5V	IN_5		
+5V	+5V	GND	IN_6		
+5V	+5V	+5V	IN_7		

1. In figure 7-5, what are the purposes of R_3 and C_1?
2. In figure 7-7, what are purposes of SW_1, SW_2 and SW_3?
3. In experiment I, what are the unadjustable errors of ADC0804 ?
4. In experiment 2, what are the unadjustable errors of ADC0809 ?

Digital to Analog Converter

Curriculum Objectives

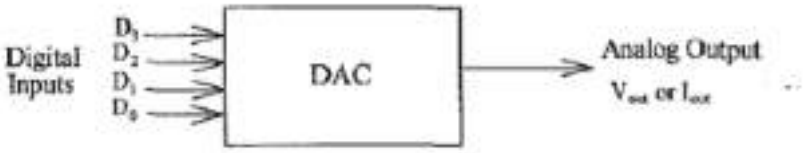
1. To understand the basic theory of digital to analog converter.
2. To understand the operation theory and characteristics of DAC0S00.
3. To generate the unipolar and bipolar analog voltage by using DAC0S00.

Curriculum Theory

Digital to analog converter (DAC) is a device, which converts the digital signal to analog signal. We normally store a digital signal in a media or transmission line. Then a DAC changes the digital signal to an analog signal in order to control data display or further analog signal processing. For example, from a digital communication system, when a receiver receives the digital modulation signal, then after via a demodulator and decoder, we can obtain the digital signal, and follow by using DAC to convert this digital signal to the analog signal. Next we will discuss the basic operation theory of DAC.

1. The Basic Theory of Digital to Analog Converter

Basically, DAC is a digital code that represents digital value converted to analog voltage or current. Figure 8-l(a) is a general 4-bit DAC binary codes, the digital input terminal D_3, D_2, D_1 and D_o are manipulated by the register in a digital system, The 4-bit code represents $2^4 = 16$ groups of 2 binary value, as shown in figure 8-l(b), For every binary code input, DAC will output a voltage (V_{out}) , which is double or other order of the binary value, According to this, analog output voltage Vout and the digital input binary values are the equivalent. If the DAC output is current, I_{out}, the theory is similarly,



D3	D2	D1	Do	Vout	D3	D2	D1	Do	Vout
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

(b)

Figure 8-1 (a) 4-bit DAC binary codes; (b) Truth table.

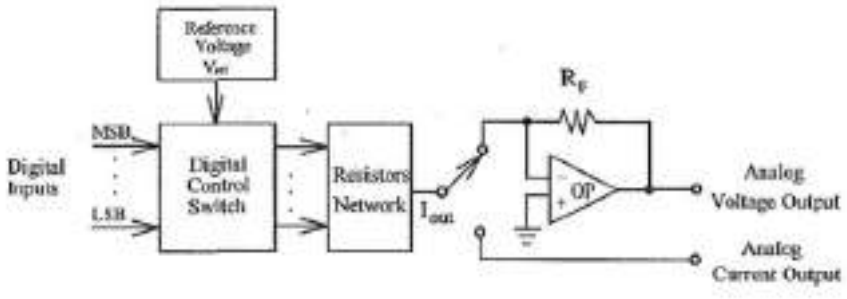


Figure 8-2 The basic block diagram of DAC.

Figure 8-2 is the basic block diagram of DAC. The reference voltage (V_{ref}) connects to the resistors network, which the digital input codes is used to control the different switch and is decided whether the V_{ref} connects with resistors network or not. Normally, the DAC analog output is represented by current, if we want to obtain the voltage output, we need to-connect an operational amplifier.

The resistors network are the main structure of DAC circuit, the most common circuits are the binary-weighted resistor converter and R-2R ladder resistors network. But the disadvantage of the binary-weighted resistor converter is the resistor value range is too large. Due to the high accuracy demand, this wide range resistor value is difficult to implement, especially for the implementation of integrated circuit (IC), which is a big problem. But for the R-2R ladder resistors network, it just needs two resistor values, which are R and 2R resistors. The resistor values are simple and just twice

of the relation, therefore, it is easy to implement in integration circuit (IC). This chapter uses the digital to analog converter DAC0800 resistors network, which is the R-2R ladder resistors network, therefore, we will discuss the theory ofR-2R ladder resistors network in next section.

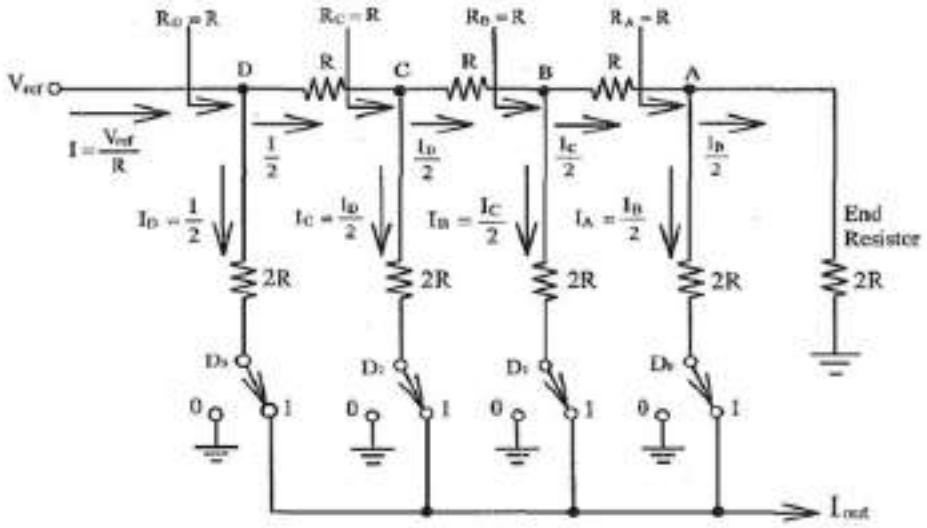


Figure 8-3 The circuit diagram of DAC with 4-bit R-2R ladder resistor network.

Figure 8-3 is the circuit diagram of DAC with 4-bit R-2R ladder resistors network, the characteristics of this circuit are no matter from A, B, C or D, the impedances are similarly. According to these characteristics, we can obtain the output current as

$$I = V_{ref}/R \qquad (8\text{-}1)$$

$$I_o = I/2$$

$$I_C = I_O/2 = I/4$$

$$I_B = I_C/2 = I/8$$

$$I_A = I_B/2 = I/16$$

$$I_{out} = I_3 + I_2 + I_B + I_A = I\left(\frac{D_3}{2} + \frac{D_2}{4} + \frac{D_1}{8} + \frac{D_0}{16}\right) \qquad (8\text{-}2)$$

Where D_3,D_2,D_1 and D_o can be divided into 1 or 0, if the switch is ON, then 1, otherwise is 0, So, we just need to control the values of D_3, D_2, D_1 and D_o correctly, then we can get the required output current I_{out}

2. Input Weight

Input weight illustrates that from the DAC digital input, when only one of the bits is 1 and the other bits are 0, the DAC output signal range is called input weight, From Figure 8-l(a), if every time we let one of the bits of D_3, D_2, D_1 and D_o as high level, the other bits is zero level, then the power of

lowest bit D_o is 1 V, D_1 is 2 V, D_2 is 4 V, D_3 is 8 V, For every bit, the input weight starts from the

lowest bit and then increases by following the weight. So we can say that V_{out} is the sum of weight of the digital input, For example, to find the V_{out} of digital input 0111, we can sum D_2, D_1 and D_o bits weight and the total value is $4+2+1=7$ V

3. Resolution and Step Size

The resolution of DAC illustrates that when the digital input terminal changes a unit, it will produce a small change at the analog output terminal, which is normally the LSB levels. Refer to figure 8-l(b), when the digital input value changes a unit, V_{out} will change at least 1 V, so the resolution is 1 V.

Resolution is also called step size because V_{out} will change, when the digital input step varies from one to another. Figure 8-4 shows a 4-bit binary counter as DAC digital input signal, the counter has a clock input, so it can output 16 types of statuses continuously in cycle. The output waveform of DAC is every step with 1V change. When the counter generates **1111,** the DAC output is the maximum value, which is 15 V. We call this situation as full-scale output. When the counter generates 0000, the DAC output is 0 V. Resolution or step size is to indicate the difference between two steps. For example, if the step size is 1 V then the difference between the steps is IV.

Figure 8-4 shows 16 types digital inputs corresponding to the 16 levels of output steps waveform. From 0 V to 15 V (full-scale), there are only 15 steps size. Generally, N bits of DAC will produce 2^N different and 2^N-l steps size.

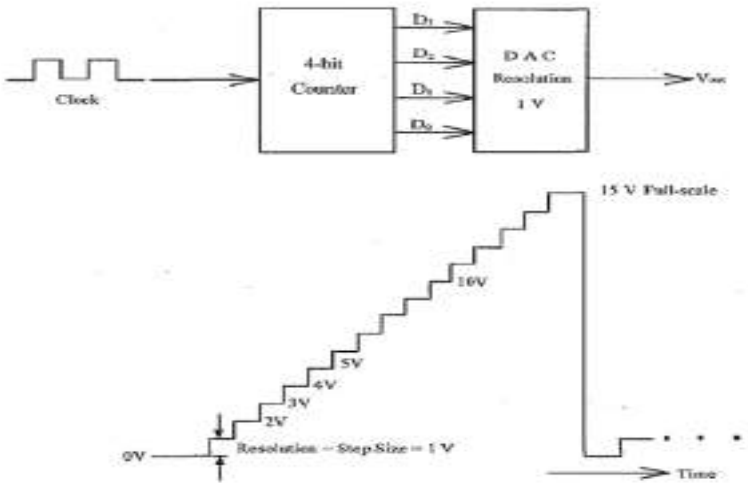


Figure 8-4 The input of DAC output waveform by using the binary counter.

4. DAC 0800 Digital to Analog Converter

DAC 0800 is a cheap and commonly used 8-bit DAC, the internal circuit consists of reference voltage power supply, R-2R ladder resistors network and transistor switch. The voltage power supply range is between ± 4.5 V to ± 18 V, under the ± 5 V condition, the power loss isapproximately 33 mW and the settling time is approximately 85 ns. Figure 8-5 is the pins diagram of DAC0800.

Figure 8-6 is the circuit diagram of DAC0800 single polarity voltage output, which D ~ D are the 8-bit digital inputs. The positive reference voltage is + 5V and passes through R1 to connect to $V_{ref}(+)$ (pin 14). The negative reference voltage is GND and passes through R2 to connect to $V_{ref}(-)$ (pin 15). The reference current I_{ref} that passes through R_1 can be expressed as

$$I_{ref} = \frac{V_{ref}}{R_1} \qquad (8\text{-}3)$$

At the current output terminal (pin 4), the output current I_{out} 1s

$$I_{out} \approx \frac{V_{ref}}{R_1}\left(\frac{D_7}{2}+\frac{D_6}{4}+\frac{D_5}{8}+\frac{D_4}{16}+\frac{D_3}{32}+\frac{D_2}{64}+\frac{D_1}{128}+\frac{D_0}{256}\right) \qquad (8\text{-}4)$$

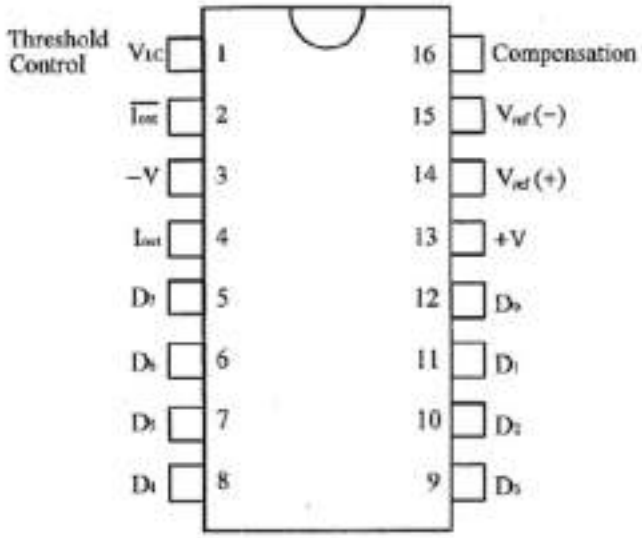


Figure 8-5 The pins diagram of DAC 0800.

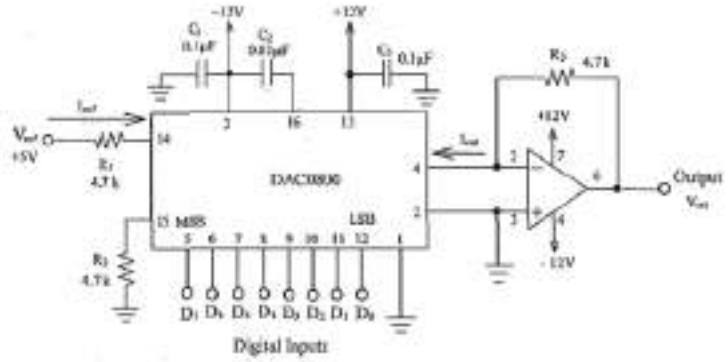


Figure 8-6 The circuit diagram ofDAC0800 single polarity voltage output.

The objective to let lout connects to µA741 is to convert the current output into the voltage output. In figure 8-6, the output voltage (V_{out}) of µA741 is

$$V_{out} = I_{out} R_1 \qquad (8\text{-}5)$$

Figure 8-7 is the circuit diagram of bipolar output voltage of DAC0800, the main different of figure 8-6 unipolar output voltage is the connection of the I_{out} output terminal (pin 2) to µA741 positive input terminal (V_{in}^{+}), so the output voltage (V_{out}) ofµA741 is

$$V_{out} = (I_{out} - I_{out}) R_1 \qquad (8\text{-}6)$$

Where I_{out} and $\overline{I}_{out}$ is the complementary output current, $I_{out} + \overline{I}_{out}$ is the full-scale current I_{FS}, then

$$I_{out} = I_{FS} - I_{out} \qquad (8\text{-}7)$$

Substituting equation (8-7).into equation (8-6), we get

$$V_{out} = 2\ I_{out}\ R_4 - I_{fs}\ R_4 \qquad (8\text{-}8)$$

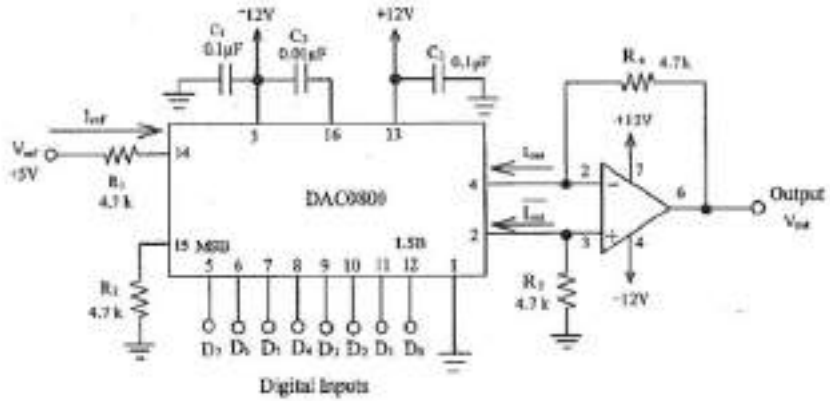


Figure 8-7 The circuit diagram of bipolar output voltage ofDAC0800

IFS = I_{out} +I_{out} where I_{out} and lout are in complementary relation,so when I_{out} equals I_{Fs}, I_{out} is zero. When I_{out} is zero, then l_{out} is I_{Fs}. From the above mentioned and equation (8-8), we know that the maximum value of V_{out} of the bipolar output voltage circuit is hsR_4 and the minimum value is the negative $I_{Fs}R_4$ Besides DAC0800, there are many types of DAC in the market, such as DAC0808 and etc. The theory and usage are almost the same, if interested, you can refer to related books.

Experiment 1: DAC0800 unipolar voltage output

I. Refer to figure 8-6 or ETEK DA-2000-04 module, let J1 short circuit, that means the l_{out} output terminal (pin 4) of DAC0800 is connected to V; input terminal (pin 2) ofμA741.

2. Calculate the step size and record the calculation in table 8-1.

3. In table 8-1, the binary values are used as the digital inputs, which " 0 " represents GND, " 1 " represents $+5\,V$.

4. Using equation (8-4) and equation (8-5) to calculate the theoretical values output current lout and output voltage V_{out}, then record in calculation in table 8-1.

5. Let J1 open circuit, that means the I_{OUT} output terminal ofDAC0800 is disconnected from V; input terminal of μA741. Then let the digital current meter connects to J1 for measuring the output current I_{out}. Then observe on the output of digital current meter and record the measured results in table 8-1.

6. Remove the current meter and let J1 short circuit. Using digital voltage meter to measure the output voltage (V_{out}) of μA741 which is pin-6. Then observe on the output of digital voltage meter and record the measured results in table 8-1.

Adjust the on/off of D_7 to D_0, input the binary values in accordance with the binary values in table 8-1. Then repeat step 5 and step 6.

Experiment 2: DAC0800 bipolar voltage output

1. Refer to figure 8-7 or ETEK DA-2000-04 module, let JI and J2 short
2. circuit, that means the lout output terminal (pin 4) of DAC0800
3. connects to the V^-_{in} output terminal (pin 2) ofμA741 and I_{out} output
4. terminal (pin 2) connects to the v^+_{in} input terminal (pin 3) ofμA741.
5. Calculate the step values and record the calculation in table 8-2.
6. In table 8-2, the binary values are used as the digital input, which "0"
7. represents GND, "1" represents +5V.
8. Using equation (8-4) to calculate I_{out} and I_{Fs}, then substitute lout and I_{Fs} into equation (8-8). Find the theoretical value of output voltage V_{out}, finally record the measured results in table 8-2. (note: when D0 to D_7 is 1, $I_{out}= I_{Fs}$)
9. Let JI and J2 short circuit. Using digital voltage meter to measure the output voltage Vout, then record the measured results in table 8-2.
10. Let JI open circuit, J2 short circuit. Connect the digital current meter to
11. JI, then measure the output current I_{out} . Observe on the output ofdigital current meter and record the measured results in table 8-2.
12. Let J2 open circuit, JI short circuit. Connect the digital current meter on J2 to measure the output current I_{out}. Observe on the output of digital current meter and record the measured results in table 8-2.
13. Calculate $I_{out} + \overline{I_{out}}$ and record the measured results in table 8-2.

Adjust the on/off of D_7 to D_0, input the binary values in accordance with the binary value in table 8-2, Then repeat step 5 and step 8.

Measured Results

Table 8-1 The measured results of unipolar voltage output ofDAC0800.

Step Size=_____

Digital Inputs								Analog Outputs			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	**Vout**		**Iout**	
								Theoretical Results	Measured Results	Theoretical Results	Measured Results
0	0	0	0	0	0	0	0				
0	0	0	0	0	0	0	1				
0	0	0	0	0	0	1	0				
0	0	0	0	0	1	0	0				
0	0	0	0	**1**	0	0	0				
0	0	0	1	0	0	0	0				
0	0	1	0	0	0	0	0				
0	1	0	0	0	0	0	0				
1	0	0	0	0	0	0	0				
1	1	1	1	1	1	1	1				

Voltage unit : V Current unit : rnA

Table 8-2 The measured results of bipolar voltage output of DAC0800.

Step Size=_____

Digital Inputs	Analog Outputs				
$D_7D_6D_5D_4D_3D_2D_1D_0$	Theoretical Results	Measured Results			
	Vout	**Vout**	**Iout**	**-Iout**	**Iout - Iout**
0 0 0 0 0 0 0 0					
0 0 0 0 0 0 **1** 0					
0 0 0 0 1 0 0 0					
0 0 1 0 0 0 0 0					
0 1 **1** **1** **1** 1 1 **1**					
1 0 0 0 0 0 0 0					
1 0 0 0 0 0 **1** 0					
1 0 0 0 **1** 0 0 0					
1 0 **1** 0 0 0 0 0					
1 **1** 0 0 0 0 0 0					
1 **1** **1** 1 **1** **1** 1 1					

Voltage unit: V Current Unit: mA

Problems Discussion

I. In experiment 1, if the digital input signal is 01101010, then what is the output voltage?

2. Try to use the step value and the output voltage range to compare the differences between the DAC0800 unipolar voltage output and bipolar voltage output.

3. According to the measured results in table 8-2, what 1s th- complementary current output (i.e. the relationship of Iout, and Iout)?

4. To understand the basic theory of digital to analog converter.

5. To understand the operation theory and characteristics of DAC0S00.

6. To generate the unipolar and bipolar analog voltage by using DAC0S00.

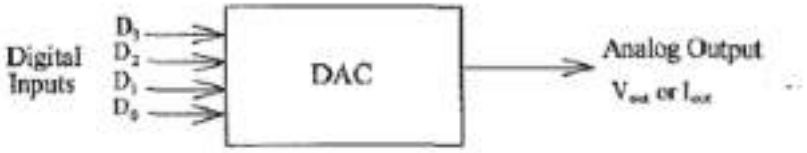
Curriculum Theory

Digital to analog converter (DAC) is a device, which converts the digital signal to analog signal. We normally store a digital signal in a media or transmission line. Then a DAC changes the digital signal to an analog signal in order to control data display or further analog signal processing. For example, from a digital communication system, when a receiver receives the digital modulation signal, then after via a demodulator and decoder, we can obtain the digital signal, and follow by using DAC to convert this digital signal to the analog signal. Next we will discuss the basic operation theory of DAC.

5. The Basic Theory of Digital to Analog Converter

Basically, DAC is a digital code that represents digital value converted to analog voltage or current. Figure 8-l(a) is a general 4-bit DAC binary codes, the digital input terminal D_3, D_2, D_1 and D_o are manipulated by the register in a digital system, The 4-bit code represents $2^4 = 16$ groups of 2 binary value, as shown in figure 8-l(b), For every binary code input, DACwill output a voltage (V_{out}) , which is double or other order of the binary value, According to this, analog

output voltage Vout and the digital input binary values are the equivalent. If the DAC output is current, I_{out}, the theory is similarly,



D3	D2	D1	Do	Vout	D3	D2	D1	Do	Vout
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	10
0	0	1	1	3	1	0	1	1	11
0	1	0	0	4	1	1	0	0	12
0	1	0	1	5	1	1	0	1	13
0	1	1	0	6	1	1	1	0	14
0	1	1	1	7	1	1	1	1	15

(b)

Figure 8-1 (a) 4-bit DAC binary codes; (b) Truth table.

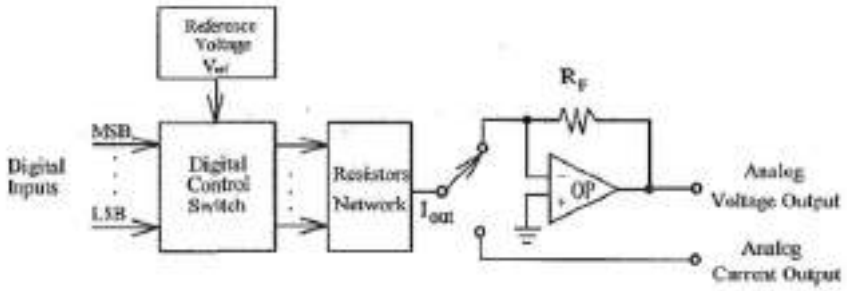


Figure 8-2 The basic block diagram of DAC.

Figure 8-2 is the basic block diagram of DAC. The reference voltage (V_{ref}) connects to the resistors network, which the digital input codes is used to control the different switch and is decided whether the V_{ref} connects with resistors network or not. Normally, the DAC analog output is represented by current, if we want to obtain the voltage output, we need to-connect an operational amplifier.

The resistors network are the main structure of DAC circuit, the most common circuits are the binary-weighted resistor converter and R-2R ladder resistors network. But the disadvantage of the binary-weighted resistor converter is the resistor value range is too large. Due to the high accuracy demand, this wide range resistor value is difficult to implement, especially for the implementation of integrated circuit (IC), which is a big problem. But for the R-2R ladder resistors network, it just needs two resistor values, which are R and 2R resistors. The resistor values are simple and just twiceof the relation, therefore, it is easy to implement in integration circuit (IC). This chapter uses the digital to analog converter DAC0800 resistors network, which is the R-2R ladder resistors network, therefore, we will discuss the theory ofR-2R ladder resistors network in next section.

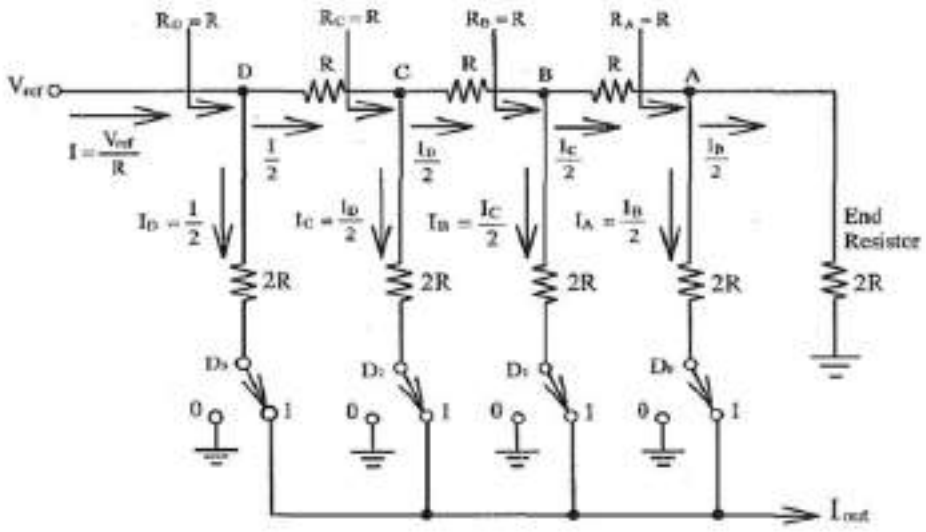


Figure 8-3 The circuit diagram of DAC with 4-bit R-2R ladder resistor network.

Figure 8-3 is the circuit diagram of DAC with 4-bit R-2R ladder resistors network, the characteristics of this circuit are no matter from A, B, C or D, the impedances are similarly. According to these characteristics, we can obtain the output current as

$$I = V_{ref}/R \qquad (8\text{-}1)$$

$$I_o = I/2$$

$$I_D = I_o/2 = I/4$$

$$I_C = I_D/2 = I/8$$

$$I_B = I_C/2 = I/16$$

$$I_{out} = I_3 + I_2 + I_1 + I_0 = I\left(\frac{D_3}{2} + \frac{D_2}{4} + \frac{D_1}{8} + \frac{D_0}{16}\right) \qquad (8\text{-}2)$$

Where D_3,D_2,D_1 and D_o can be divided into 1 or 0, if the switch is ON, then 1, otherwise is 0, So, we just need to control the values of D3, D2, D_1 and D_o correctly, then we can get the required output current I_{out}

6. Input Weight

Input weight illustrates that from the DAC digital input, when only one of the bits is 1 and the other bits are 0, the DAC output signal range is called input weight, From Figure 8-l(a), if every time we let one of the bits of D_3, D_2, D_1 and D_o as high level, the other bits is zero level, then the power of

lowest bit D_o is 1 V, D_1 is 2 V, D_2 is 4 V, D_3 is 8 V, For every bit, the input weight starts from the lowest bit and then increases by following the weight. So we can say that V_{out} is the sum of weight of the digital input, For

example, to find the V_{out} of digital input 0111, we can sum D_2, D_1 and D_o bits weight and the total value is $4+2+1=7$ V

7. Resolution and Step Size

The resolution of DAC illustrates that when the digital input terminal changes a unit, it will produce a small change at the analog output terminal, which is normally the LSB levels. Refer to figure 8-l(b), when the digital input value changes a unit, V_{out} will change at least 1 V, so the resolution is 1 V.

Resolution is also called step size because V_{out} will change, when the digital input step varies from one to another. Figure 8-4 shows a 4-bit binary counter as DAC digital input signal, the counter has a clock input, so it can output 16 types of statuses continuously in cycle. The output waveform of DAC is every step with 1V change. When the counter generates **1111,** the DAC output is the maximum value, which is 15 V. We call this situation as full-scale output. When the counter generates 0000, the DAC output is 0 V. Resolution or step size is to indicate the difference between two steps. For example, if the step size is 1 V then the difference between the steps is IV.

Figure 8-4 shows 16 types digital inputs corresponding to the 16 levels of output steps waveform. From 0 V to 15 V (full-scale), there are only 15 steps size. Generally, N bits of DAC will produce 2^N different levels and 2^N-l steps size.

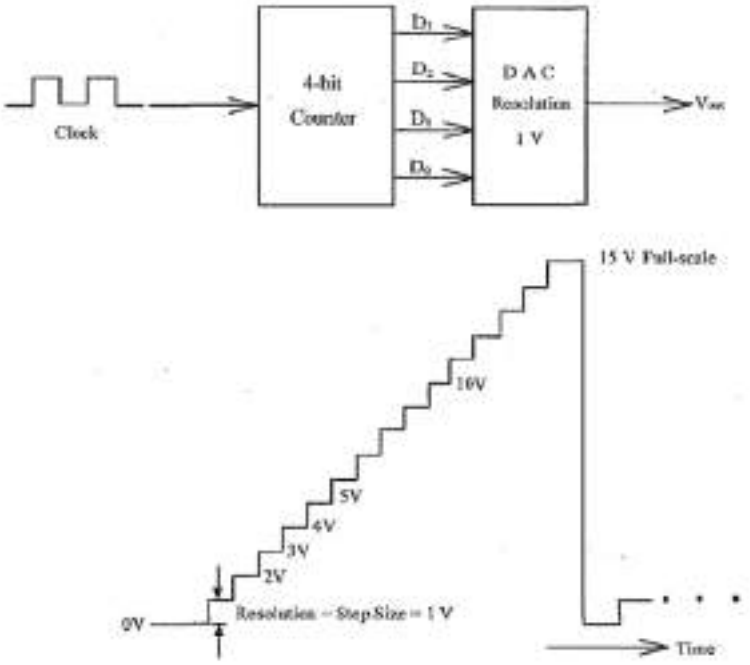


Figure 8-4 The input of DAC output waveform by using the binary counter.

8. DAC 0800 Digital to Analog Converter

DAC 0800 is a cheap and commonly used 8-bit DAC, the internal circuit consists of reference voltage power supply, R-2R ladder resistors network and transistor switch. The voltage power supply range is between ± 4.5 V to ± 18 V, under the ± 5 V condition, the power loss is approximately 33 mW and the settling time is approximately 85 ns. Figure 8-5 is the pins diagram of DAC0800.

Figure 8-6 is the circuit diagram of DAC0800 single polarity voltage output, which $D_7 \sim D_0$ are the 8-bit digital inputs. The positive reference voltage is + 5V and passes through R1 to connect to $V_{ref}(+)$ (pin 14). The negative reference voltage is GND and passes through R2 to connect to $V_{ref}(-)$ (pin 15). The reference current I_{ref} that passes through R_1 can be expressed as

$$I_{ref} = \frac{V_{ref}}{R_1} \qquad (8\text{-}3)$$

At the current output terminal (pin 4), the output current I_{out} 1s

$$I_{out} \approx \frac{V_{ref}}{R_1}\left(\frac{D_7}{2}+\frac{D_6}{4}+\frac{D_5}{8}+\frac{D_4}{16}+\frac{D_3}{32}+\frac{D_2}{64}+\frac{D_1}{128}+\frac{D_0}{256}\right) \qquad (8\text{-}4)$$

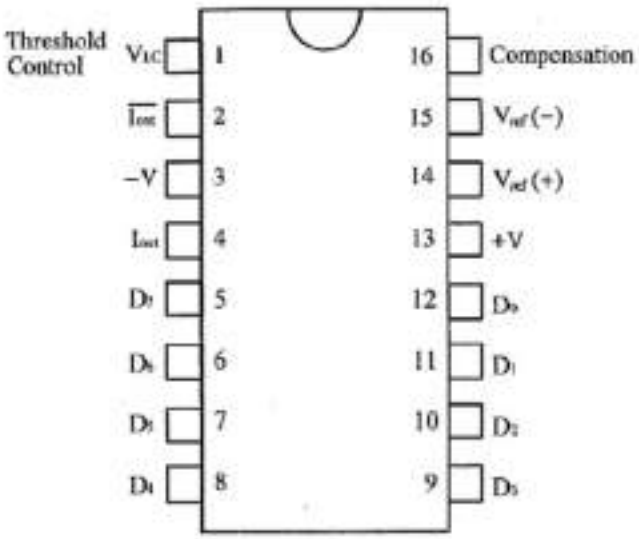


Figure 8-5 The pins diagram of DAC 0800.

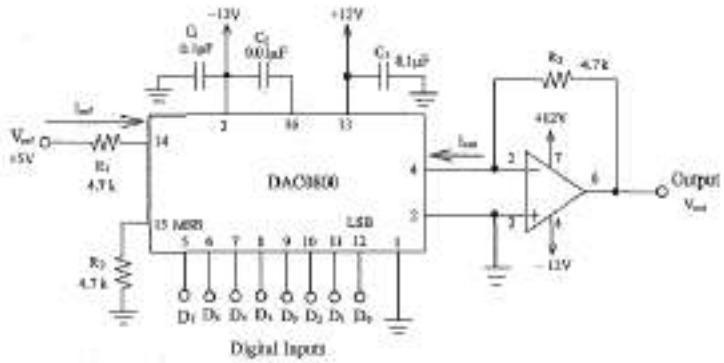


Figure 8-6 The circuit diagram ofDAC0800 single polarity voltage output.

The objective to let lout connects to µA741 is to convert the current output into the voltage output. In figure 8-6, the output voltage (V_{out}) of µA741 is

$$V_{out} = I_{out} R_f \qquad (8\text{-}5)$$

Figure 8-7 is the circuit diagram of bipolar output voltage of DAC0800, the main different of figure 8-6 unipolar output voltage is the connection of the I_{out} output terminal (pin 2) to µA741 positive input terminal (V_{in}^{+}), so the output voltage (V_{out}) ofµA741 is

$$V_{out} = (I_{out} - I_{out}) R_f \qquad (8\text{-}6)$$

Where I_{out} and $I_{\overline{out}}$ is the complementary output current, $I_{out} + I_{\overline{out}}$ is the full-scale current I_{FS}, then

$$I_{out} = I_{FS} - I_{out} \qquad (8\text{-}7)$$

Substituting equation (8-7).into equation (8-6), we get

$$V_{out} = 2\ I_{out}\ R_4 - I_{fs}\ R_4$$

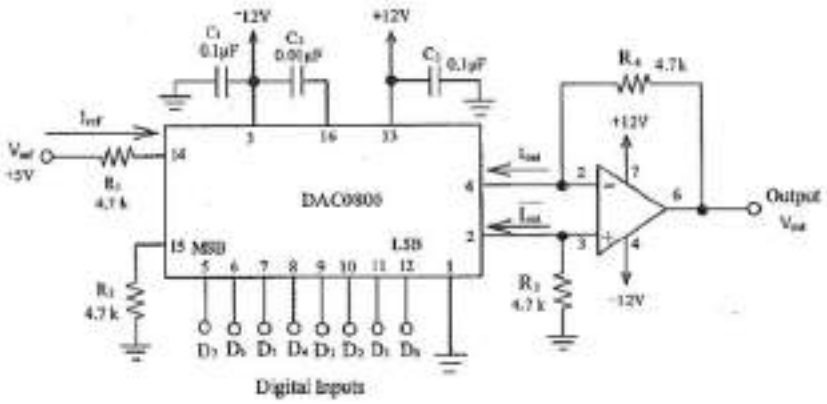


Figure 8-7 The circuit diagram of bipolar output voltage ofDAC0800

IFS = I_{out} +I_{out} where I_{out} and lout are in complementary relation, so when I_{out} equals I_{Fs}, I_{out} is zero. When I_{out} is zero, then l_{out} is I_{Fs}. From the above mentioned and equation (8-8), we know that the maximum value of V_{out} of the bipolar output voltage

circuit is hsR_4 and the minimum value is the negative $I_{Fs}R_4$ Besides DAC0800, there are many types of DAC in the market, such as **DAC0808** and etc. The theory and usage are almost the same, if interested, you can refer to related books.

Experiment 1: DAC0800 unipolar voltage output

1. Refer to figure 8-6 or ETEK DA-2000-04 module, let J1 short circuit, that means the l_{out} output terminal (pin 4) of DAC0800 is connected to V; input terminal (pin 2) ofμA741.
2. Calculate the step size and record the calculation in table 8-1.
3. In table 8-1, the binary values are used as the digital inputs, which " 0 " represents GND, " 1 " represents $+5\,V$.
4. Using equation (8-4) and equation (8-5) to calculate the theoretical values output current lout and output voltage V_{out}, then record in calculation in table 8-1.
5. Let J1 open circuit, that means the I_{OUT} output terminal ofDAC0800 is disconnected from V; input terminal of μA741. Then let the digital current meter connects to J1 for measuring the output current I_{out} . Then observe on the output of digital current meter and record the
1. measured results in table 8-1.
6. Remove the current meter and let J1 short circuit. Using digital voltage meter to measure the output voltage (V_{out}) of μA741 which is pin-6. Then observe on the output of digital voltage meter and record the measured results in table 8-1.

Adjust the on/off of D_7 to D_0, input the binary values in accordance with the binary values in table 8-1. Then repeat step 5 and step 6

Experiment 2: DAC0800 bipolar voltage output

1. Refer to figure 8-7 or ETEK DA-2000-04 module, let JI and J2 short
i. circuit, that means the lout output terminal (pin 4) of DAC0800
ii. connects to the V^-_{in} output terminal (pin 2) ofμA741 and I_{out} output
iii. terminal (pin 2) connects to the v^+_{in} input terminal (pin 3) ofμA741.
2. Calculate the step values and record the calculation in table 8-2.

3. In table 8-2, the binary values are used as the digital input, which "0"
i. represents GND, "1" represents +5V.

4. Using equation (8-4) to calculate I_{out} and I_{Fs}, then substitute lout and I_{Fs} into equation (8-8). Find the theoretical value of output voltage V_{out}, finally record the measured results in table 8-2. (note: when D0 to D_7 is 1, $I_{out} = I_{Fs}$)

5. Let JI and J2 short circuit. Using digital voltage meter to measure the output voltage Vout, then record the measured results in table 8-2.

6. Let JI open circuit, J2 short circuit. Connect the digital current meter to
i. JI, then measure the output current I_{out} . Observe on the output ofdigital current meter and record the measured results in table 8-2.

7. Let J2 open circuit, JI short circuit. Connect the digital current meter on J2 to measure the output current I_{out}. Observe on the output of digital current meter and record the measured results in table 8-2.

8. Calculate $I_{out} + \overline{I_{out}}$ and record the measured results in table 8-2.

Adjust the on/off of D_7 to D_0, input the binary values in accordance with the binary value in table 8-2, Then repeat step 5 and step 8.

Measured Results

Table 8-1 The measured results of unipolar voltage output ofDAC0800.

Step Size=_____

Digital Inputs								Analog Outputs			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	**Vout**		**Iout**	
								Theoretical Results	Measured Results	Theoretical Results	Measured Results
0	0	0	0	0	0	0	0				
0	0	0	0	0	0	0	1				
0	0	0	0	0	0	1	0				
0	0	0	0	0	1	0	0				
0	0	0	0	**1**	0	0	0				
0	0	0	1	0	0	0	0				
0	0	1	0	0	0	0	0				
0	1	0	0	0	0	0	0				
1	0	0	0	0	0	0	0				
1	1	1	1	1	1	1	1				

Voltage unit : V Current unit : rnA

Table 8-2 The measured results of bipolar voltage output of DAC0800.

Step Size=_____

Digital Inputs	Analog Outputs				
$D_7D_6D_5D_4D_3D_2D_1D_0$	Theoretical Results	Measured Results			
	Vout	**Vout**	**Lout**	**-lout**	**lout + -lout**
0 0 0 0 0 0 0 0					
0 0 0 0 0 0 **1** 0					
0 0 0 0 1 0 0 0					
0 0 1 0 0 0 0 0					
0 1 **1** **1** **1** 1 1 **1**					
1 0 0 0 0 0 0 0					
1 0 0 0 0 0 **1** 0					
1 0 0 0 **1** 0 0 0					
1 0 **1** 0 0 0 0 0					
1 **1** 0 0 0 0 0 0					
1 **1** **1** 1 **1** **1** 1 1					

Voltage unit: V Current Unit: mA

ASK Modulation

Curriculum Objectives

I. To understand the operation theory of the amplitude shiftkeying (ASK) modulation.

2. To understand the signal waveform of the ASK modulation.

3. To implement the ASK modulator by using MC1496.

4. To understand the methods of testing and adjusting the ASKmodulation circuit.

Curriculum Theory

In the wireless digital communication, it is not easy to transmit the digital data directly. This is because it needs to pass through the modulator and modulate the carrier signal in order to send the signal effectively. One of the easiest ways is to use the different data stream to change the amplitude of carrier, this kind of modulation is called amplitude modulation, and we call it as amplitude shift keying (ASK) modulation in digital communication.

ASK modulation signal can be expressed as

$$x_{ASK}(t) = A\cos(\omega_c t + \phi_0); \quad 0 < t < T, i = 1, 2, \cdots, M \qquad (11\text{-}1)$$

In equation **(11-1),** the values of amplitude A, have M types of possible change, the ω_c, and ϕ_0 denote the cutoff frequency and phase, respectively. If we choose M = 2 , the X ASK (t) signal will transmit the binary signal, therefore, the values of A are $A_1 = 0$ and $A_2 = A$, A is the arbitrary constant so we can obtain the binary ASK modulated signal waveform as shown in figure 11-1. When input logic is **1,** then the signal is transmitted out; when the input logic is 0, then no signal is transmitted, so this also called on-off keying (OOK), this type of method is used in the past time.

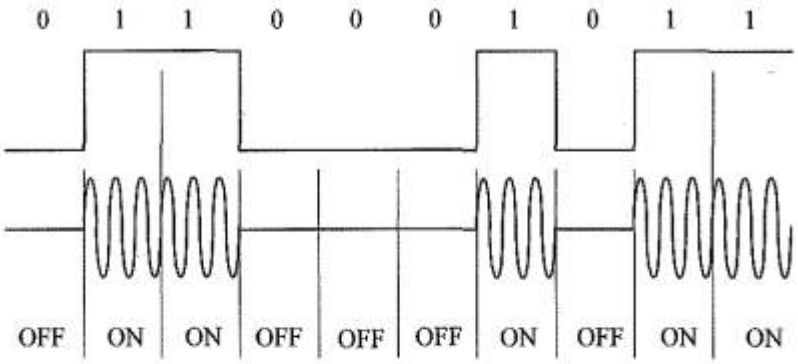


Figure 11-1 ASK modulation signal waveform.

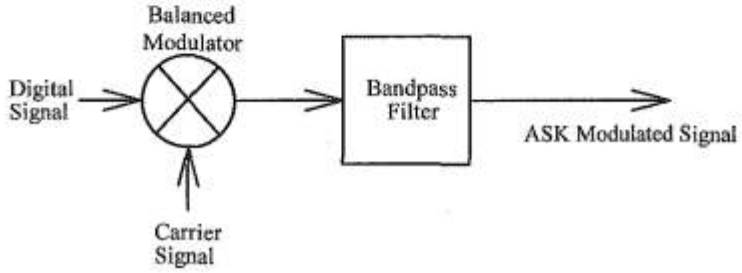


Figure 11-2 The basic block diagram of ASK modulator.

Figure 11-2 is the basic block diagram of ASK modulator, which the balanced modulator can meet the objectives of amplitude modulation, and the bandpass filter will remove the high frequency signal to make the ASK signal waveform perfectly. We use the MC1496 to implement the balanced modulator in this experiment. Figure 11-3 is the internal circuit diagram of MC1496, where D1, R1, R2, R3, Q_7 and Qs comprise a current source, it provides DC bias current to Q_5 and Q_6• The Q_5 and Q_6 comprise a differential amplifier, which is used to drive the Q_1, Q_2, Q_3 and Q_4 to become double differential amplifiers. The data signal is inputted between pin 1 and pin 4. The carrier signal is inputted between pin 8 and pin 10. The gain of balanced modulator is inputted between pin 2 and pin 3, which is controlled by the resistor between pin 2 and pin 3. The range of bias current of the amplifier is determined by the resistor connected at the pin 5.

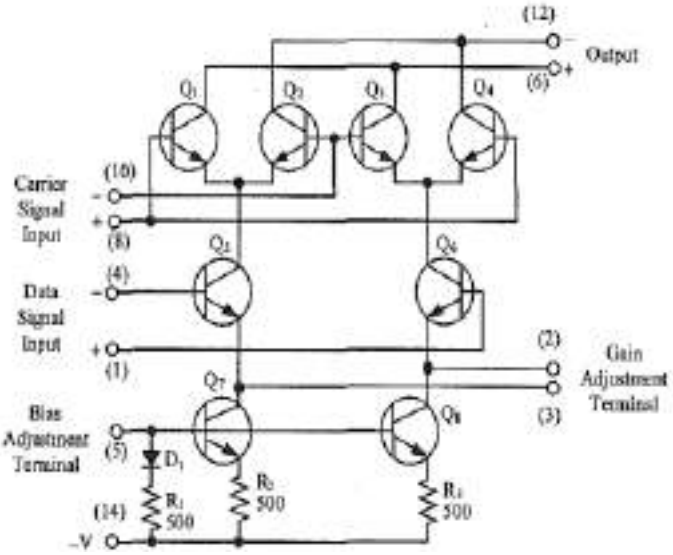


Figure 11-3 The internal circuit diagram of MC1496.

Figure 11-4 is the circuit diagram

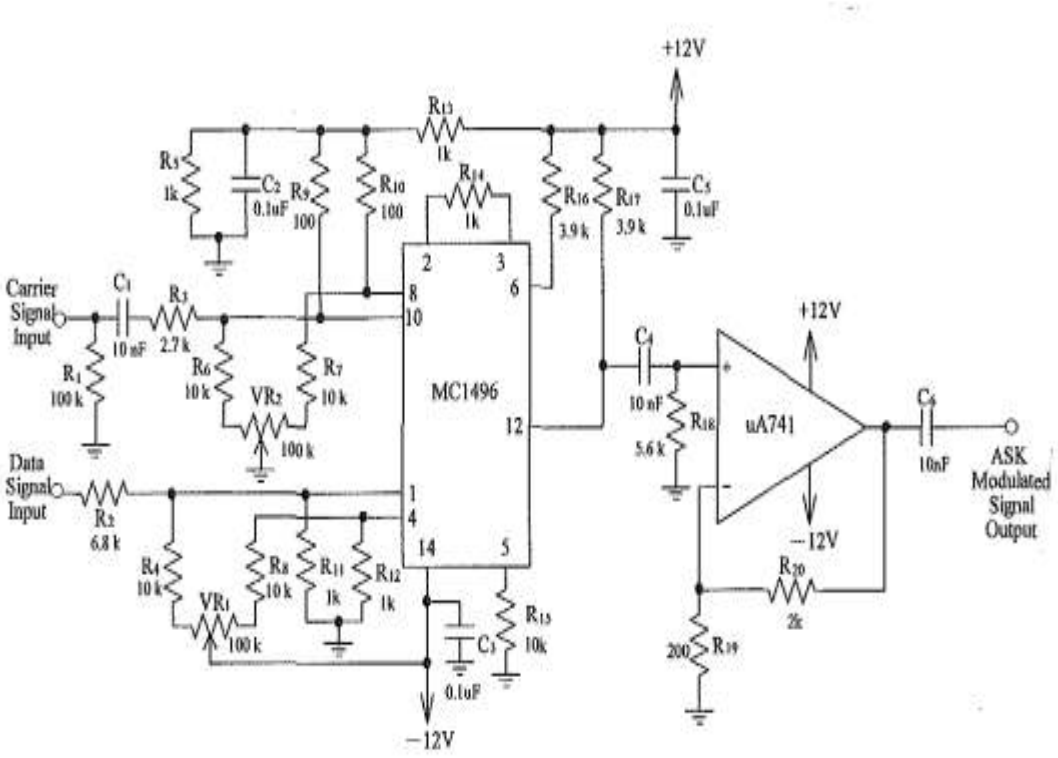


Figure 11-4 The circuit diagram of ASK modulator by using MC1496.

Experiment Items

Experiment 1: ASK modulator

1. Refer to figure 11-4 or ETEK DA-2000-06 module.
2. At the data signal input terminal, input 5 V_{PP} amplitude, 2.5 V offset (i.e. high is 5 V, low is 0 V), 100 Hz square wave frequency. Then from the carrier signal input terminal, input 800 m V_{PP} amplitude and 20 kHz sine wave frequency.
3. At the ASK modulation signal output terminal (ASK O / P), by using oscilloscope, observe on the output signal waveform. Adjust VR_1 and observe on the ASK modulated signal waveform before the waveform occurs distortion. Then adjust VR_2 to avoid the asymmetry of the signal. Finally record the output signal waveform in table 11-1.
4. Change the data signal frequency to 500 Hz and 1 kHz, the others remain the same. By using oscilloscope, observe on the output signal waveform and record the measured results in table 11-1.
5. At the data signal input terminal, input 5 V_{PP} amplitude, 2.5 V offset (i.e. high is 5 V, low is 0 V), 1 kHz square wave frequency. Then at the carrier signal input terminal input 800 m V_{PP} amplitude and 20 kHz sine wave frequency.
6. At the ASK modulation signal output terminal (ASK O / P), by using oscilloscope, observe on the output signal waveform. Adjust VR_1 and observe on the ASK modulation signal waveform before the signal waveform occurs distortion. Then adjust VR_2 to avoid the asymmetry of the signal. Finally record the output signal waveform in table 11-2.

7. Change the carrier signal frequencies to 50 kHz and I00 kHz, the others remain the same. By using oscilloscope, observe on the output signal waveform then record the measured results in table 11-2.

8. At the data signal input terminal input 5 V_{PP} amplitude, 2.5 V offset (i.e.high is 5 V, low is O V), 1 kHz square wave frequency. Then from the carrier signal input terminal input 800 m V_{PP} amplitude and 100 kHz sine wave frequency.

9. At the ASK modulation signal output terminal (ASK O / P), by using oscilloscope, observe on the output signal waveform. Adjust VR_1 and observe on the ASK modulation signal waveform before the signal waveform occurs distortion. Adjust VR_2 to avoid the asymmetry ofthe signal. Finally record the output signal waveform in table 11-3.

10. Change the carrier signal amplitudes to 1.6 V_{PP} and 2 V_{PP}, the others remain the same. By using oscilloscope, observe on the output signal waveform then record the measured results in table 11-3.

Measured Results

Table 11-1 The measured results of ASK output signal waveforms by varying thedata signal frequency (V_0= 800 m V_{PP}, f_0= 20 kHz).

Data Signal Frequencies	Data Signal Waveforms	ASK Output Signal Waveforms
100Hz		
500Hz		
1 kHz		

Table 11-2 The measured results of ASK output signal waveforms by varying thecanier signal frequency ($V_0 = 800$ m V_{PP} , $f_{Data} = 1$ kHz).

Canier Signal Frequencies	Carrier Signal Waveforms	ASK Output Signal Waveforms
20kHz	P	
50kHz		
100 kHz		

Table 11-3 The measured results of ASK output signal waveforms by varying thecarrier signal amplitude (f_0 = 100 kHz, f_{Data} = 1kHz).

Carrier Signal Amplitudes	Carrier Signal Waveforms	ASK Output Signal Waveforms
800mV_{PP}		
1.6 V_{PP}		
2 V_{PP}		

Problems Discussion

1. In figure 11-4, what are functions ofµA741, C_4,R_{18}, R_{19} and R_{20}?
2. In figure 11-4, what are the purposes of VR_1 and VR_2?
3. In figure 11-4, what are the purposes of R_{14} and R_{15}?

ASK Demodulation

1. To understand the operation theory of ASK asynchronousdetector.
2. To understand the operation theory of ASK synchronousdetector.
3. To understand the methods of testing and adjusting the ASKdemodulation circuit

Curriculum Theory

we have mentioned that we need a modulator to modulate the data to a high carrier frequency, so that the signal can be transmitted effectively. Therefore, for receiver, we must convert the digital signal back to the modulating signal. Figure 12-1 shows the theoretical diagram of ASK demodulation. There are two methods to design the ASK demodulator, which are asynchronous detector and synchronous detector. We will discuss these two types of ASK demodulator in this chapter.

1. Asynchronous ASK Detector.

The theories of ASK demodulation diode detector and the amplitude demodulator in chapter 4 are similar, please refer to chapter 4 for the AM demodulator. Figure 12-2 is the circuit diagram of asynchronous ASK
detector, which R1, R2 and U1 comprise an inverting amplifier to amplify the input signal. Then D_1 is the rectifying diode to make the modulation signal passes through D_1 half wave rectifier. R_3 and C_1 comprise a low-pass filter. U2, VR_1, D_2, Ri and C2 comprise a comparator, therefore, the output terminal can demodulate the digital demodulated signal.

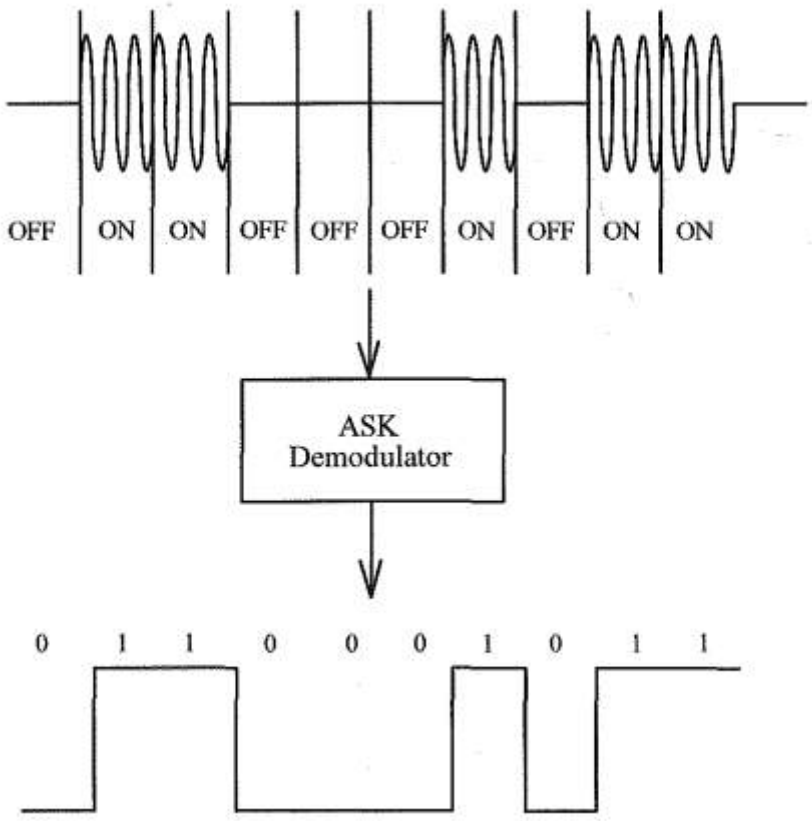


Figure 12-1 The theoretical diagram of ASK demodulation.

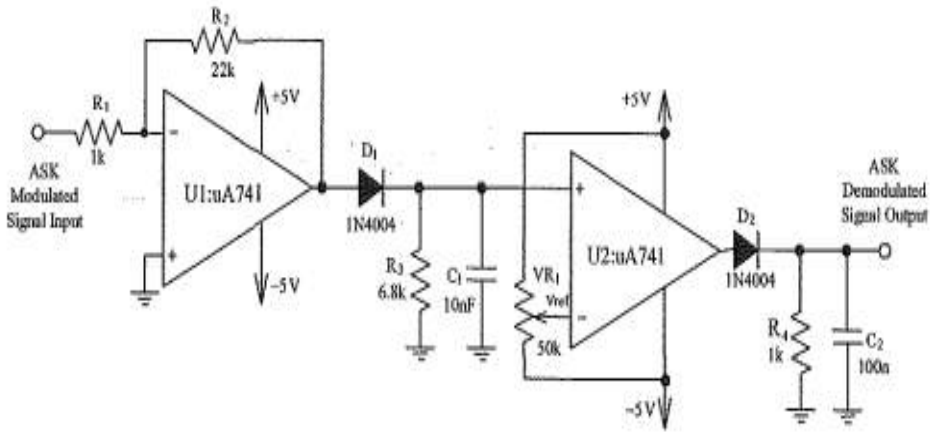


Figure 12-2 The circuit diagram of ASK asynchronous detector.

2. Synchronous ASK Detector

We have mentioned before that we can use synchronous detector to design the ASK demodulation. This experiment utilizes the square-law detector and the block diagram is shown in figure 12-3. In figure 12-3, we utilize MC1496 balanced modulator to design the square-law detector. Figure 12-4 is the internal circuit diagram ofMC1496 balanced modulator (Readers may refer to the circuit diagram in chapter 11). Let $X_{ASK}(t)$ be the ASK modulated signal, which is

$$X_{ASK}(t)=A_i \cos(\omega_c t+\phi_0); \quad 0<t>T, \quad i=l,2,\ldots,M \qquad (12\text{-}1)$$

Data Signal

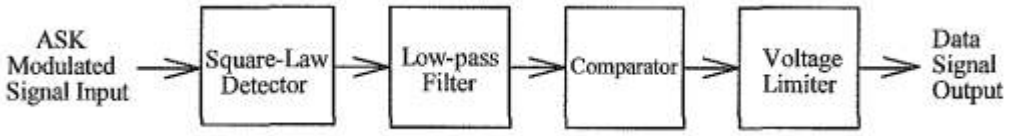


Figure 12-3 The basic block diagram of ASK demodulator

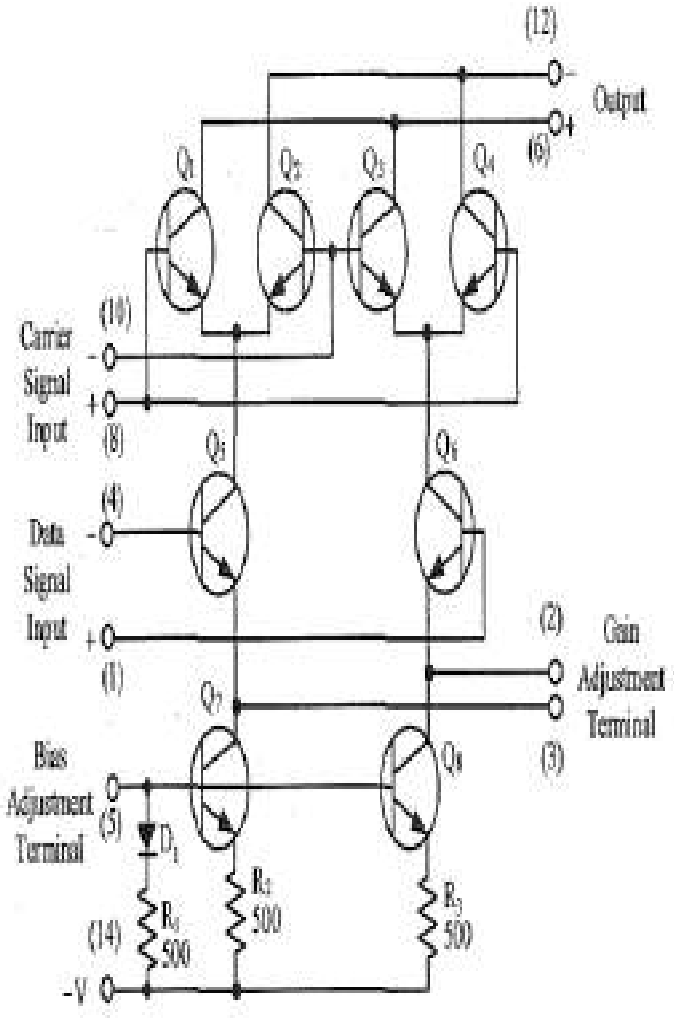


Figure 12-4 The internal circuit diagram ofMC1496 balanced modulator

In equation (12-1), the values of amplitude A, have M types of possible change, the ω_c, and ϕ_0

denote the cutoff frequency and phase constant, respectively. When we input the ASK modulated signal to the two input terminals of the balanced modulator, then the output signal of the balanced modulator can be expressed as

$$x_{out}(t) = k x_{ASK}(t)\, x_{ASK}(t) = kA_i^2 \cos^2(\omega_c + \phi_0) = \frac{kAi2}{2} + \frac{kAi2}{2}\cos(2\omega ct + 2\phi)_0$$

(12-2)

Where $0 < t < T$, $i = 1,2,\cdots,M$

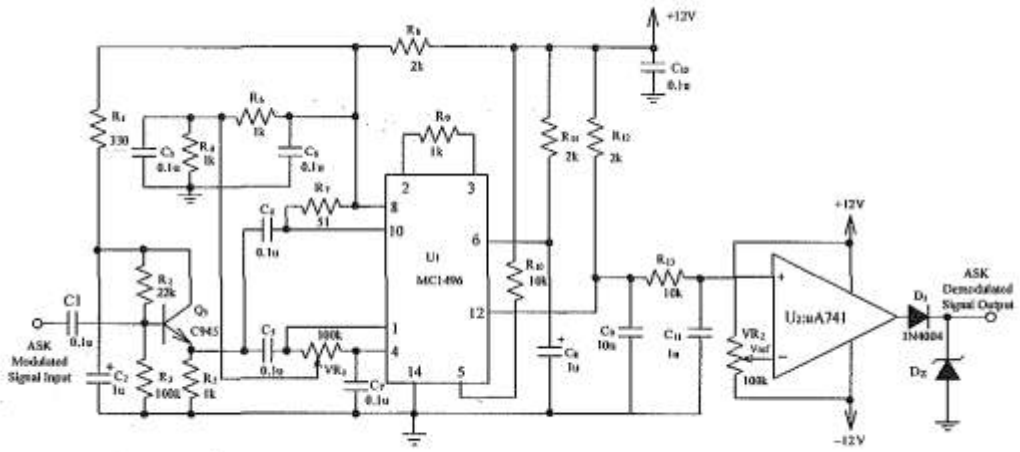


Figure 12-5 The circuit diagram of ASK synchronous detector.

where k represents the gain of the balanced modulator. The first term of equation (12-2) is the data signal amplitude and the second term is the 2nd harmonic of the modulated signal. From the output signal $X_{out}(t)$, if the first data-signal amplitude receives the demodulated ASK signal, this means that the data signal can be recovered correctly.

Figure 12-5 is the circuit diagram of the synchronous ASK detector, the structure is similar to the AM detector in the term 4. In figure 12-5, Q_1, C_1,C_2, R_2 , R_3 and R_5 comprise an emitter follower. VR_1 controls the input ranges of modulated ASK signal and the output signal ofMC1496 (pin 12) is shown in equation (12-2). The C_9, C_{11} and, R_{13} comprise a low-pass filter, which the objective is to remove the 2nd harmonic of modulated ASK signal as shown in the second term in equation (12-2). The first term in the equation (12-2) is the data signal amplitude part, which can be recovered by using the comparator and voltage limiter comprised by U_2, VR_2, D_1, and Dz.

Experiment Items

Experiment 1: Asynchronous ASK detector

1. Use the ASK modulator in chapter 11 (as shown in figure 11-4) or refer to ETEK DA-2000-06 modules to produce the amplitude modulated signal as the modulated ASK signal input.

2. At the data signal input terminal, input 5 V_{PP} amplitude, 2.5 V offset (i.e.high is 5 V and low is 0 V), and 100 Hz square wave frequency. At the carrier signal input terminal, input 800 m V_{PP} amplitude and 20 kHz sine wave frequency.

3. Adjust VR_1 of ASK modulator and observe on the modulated ASK signal before the signal occurs distortion, then slightly adjust VR_2 to avoid the asymmetry of the signal to obtain the optimum output waveform of modulated ASK signal.

4. In figure 11-4, let the ASK modulator output signal connects to the input terminal of modulated ASK signal of the asynchronous detector in figure 12-2 (ASK I/ P).

5. Change the oscilloscope to DC channel, and adjust VR_1 of figure 12-2 to obtain the optimum comparator reference voltage. Then observe onthe asynchronous detector output signal waveform and record the measured results in table 12-1.

6. Change the input data signal frequencies of the ASK modulator to 50 Hz and 200 Hz, the others remain the same, and then repeat step 5.

7. Adjust the input of ASK modulator carrier signal amplitude to 800 m V_{PP}, 100 kHz sine wave frequency. At the data signal input terminal, input 5 V_{PP} amplitude, 2.5 V offset (i.e. high is 5 V and low is 0 V) and 100 Hzsquare wave frequency.

8. Refer to figure 11-4, adjust VR_1 of ASK modulator, observe on the ASK modulator signal waveform before the waveform occurs distortion. Then slightly adjust VR_2 to avoid the asymmetry of the signal to obtain the

optimum output waveform of modulated ASK signal.

9. Change the oscilloscope to the DC channel, then adjust VR_1 of figure 12-2 to obtain the optimum comparator reference voltage. Then observe on the asynchronous detector output signal waveform and then record the measured results in table 12-2.

10. Change the output data signal frequencies of the amplitude modulator to 50 Hz and 20 Hz , the others remain the same and then repeat step 9.

Experiment 2: Synchronous ASK detector

I. Use the ASK modulator in chapter I 1 (as shown in figure 11-4) or refer to ETEK DA-2000-06 module to produce the modulated ASK signal as the modulated ASK signal input.

2. At the data signal input terminal, input 5 VPP amplitude, 2.5 V offset (i.e. high is 5 V and low is O V) and 100 Hz square wave frequency. At the carrier signal input terminal, input 800 m V_{PP} amplitude and 100 kHz sine wave frequency.

3. Adjust VR1 of ASK modulator and observe on the modulated ASK signal waveform before the waveform occurs distortion. Then slightly adjust VR_2 to avoid the asymmetry-of-the-signal to-obtain the-optimum output waveform of the modulated ASK signal.

4. Let the ASK modulator output signal connects to the input terminal of modulated ASK signal of synchronous ASK detector in figure 12-5 (ASK I/P).

5. By using oscilloscope and switching to DC channel, then adjust VR_2 of figure 12-5 to obtain the optimum comparator reference voltage. Then observe on the synchronous ASK detector output

6. signal waveform and record the measured results in table 12-3. If the signal output waveform occurs distortion, then slightly adjust VR1.

7. Change the input data signal frequencies of ASK modulator to 50 Hz and 200 Hz, the others remain the same and repeat step 5.

8. Adjust input carrier signal amplitude of ASK modulator to 800 m V_{PP} and 40 kHz sine wave frequency. At the data signal input terminal, input 5 VPP amplitude, 2.5 V offset (i.e. high is 5 V and low is 0 V) and 100 Hz square wave frequency.

9. Refer to figure 11-4, adjust VR_1 of ASK modulator and observe on the modulated ASK signal waveform before the waveform occurs distortion. Then slightly adjust VR_2 to avoid the asymmetry of the signal to obtain the optimum output waveform of the modulated ASK signal.

10. By using oscilloscope and switching to DC channel, then adjust VR_2 of figure 12-5 to obtain the optimum comparator reference voltage. Then observe on the synchronous ASK detector output signal waveform and then record the measured results in table 12-4. If the signal output waveform occurs distortion, then slightly adjust VR1.

11. Change the input carrier signal frequencies of ASK modulator to 70 kHz and 100 kHz, the others remain the same and repeat step 9.

Result

Table 12-1 The measured results of ASK demodulator by using asynchronousdetector (V_c=800mV_{PP}, f_c=20kHz).

Data Signal Frequencies	Modulated ASK Signal Waveforms	Demodulated ASK Signal Waveforms
100 Hz		
50Hz		
200Hz		

Table 12-2 The measured results of ASK demodulator by using an asynchronous detector(V_0 =800mV_{PP}, f_0=100kHz).

Data Signal Frequencies	Modulated ASK Signal Waveforms	Demodulated ASK SignalWaveforms
100 Hz		
50Hz		-
200Hz		

Table 12-3 The measured results of ASK demodulator by using a synchronous detector(V_0= 800 m V_{PP}, f_0=100 kHz).

Data Signal Frequencies	Modulated ASK Signal Waveforms	Demodulated ASK Signal Waveforms
100 Hz		
50Hz		
200Hz		

Table 12-4 The measured results of ASK demodulator by using synchronous detector (V_0 =800mV_{PP}, f_{Data}=I00Hz).

Carrier Signal Frequencies	Modulated ASK Signal Waveforms	Demodulated ASK Signal Waveforms
40kHz		
70kHz		
100 kHz		

Problems Discussion

I. In figure 12-2, if we neglect the µA741 op-amp and connect the ASKmodulator to the diode detector, then what are the results?

2. What are the purposes of the comparators in figure 12-2 and figure12-5?

3. In figure 12-5, what are the objectives of R_{13}, $C_{9,}$ and C_{11}?

4. In Figure 12-5, what are the objectives of D_1 and D_Z?

FSK Modulation

Curriculum Objectives-

1. To understand the operation theory of the FSK modulator.
2. To design and implement the FSK modulator by using VCO.

In digital signal transmission, the repeater is used to recover the datasignal, this will enhance the immunity to noise. So the coding technique can be used to detect, correct and encrypt the signal. During long-haultransmission, the high-frequency part of the digital signal will easily attenuate and cause distortion. Therefore, the signal has to be modulated before transmission, and one of the methods is the frequency-shift keying(FSK) modulation. FSK technique is to modulate the data signal to twodifferent frequencies to achieve effective transmission. At the receiver, thedata signal will be recovered based on the two different frequencies of thereceived signal. The relation of FSK signal and data signal is shown infigure 13-1. When the data signal is "high", the frequency of the FSK signal isf1, and when the data signal is "low", the frequency of the FSK signal is f_2• Normally, the difference between frequencies f_1 and f_2 has to be as large as possible. This is because the correlation of both signals is low, therefore, the effect of transmitting and receiving will.be better. However, the required bandwidth must be increased.

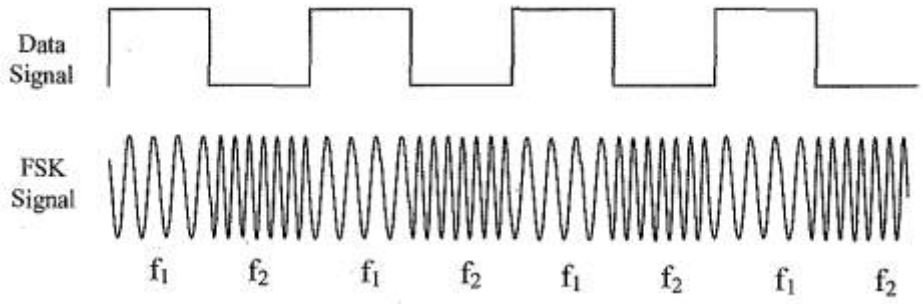


Figure 13-1 The relation diagram between data signal and FSK signal.

The technique of FSK is widely used in commercial and industrial wire transmission and wireless transmission. In the experiments, we will discuss how to--produce the FSK signal. In certain applications, the FSK signal is fixed. For example, for wireless transmission, the mark signal is 2124 Hz and the space signal is 2975 Hz. For wire transmission, the frequencies are as follow:

Space= 1270 Hz

Mark= 1070 Hz

Space = 2225 HzMark = 2025 Hz

From the above mentioned, we notice that the frequency gap of FSK is200Hz.

In FSK modulator, we use data signal (square wave) as the signal source. The output signal /frequency of the modulator is based on the square wave levels of the data signal. In this chapter, the frequencies of the carriers are 1070 Hz and 1270 Hz. These two frequencies can be produced by using a voltage-controlled oscillator, (VCO). The output signal frequencies are varied by the different levels of the input pulse to produce two different frequencies. Each output signal frequency corresponds to an input voltage level (i.e. "0" or "l ").

In this chapter, we use the LM566 voltage control oscillator to implement the FSK modulator as shown in figure 13-2. The oscillation frequency of LM566 is

$$f_r = \frac{2}{R_{10}C_5}\left(\frac{V_{cc} - V_{in}}{V_{cc}}\right) \quad (13\text{-}1)$$

Where V_{cc} is the power supply voltage input at pin 8 of LM566. Vin 1s the input voltage ofLM566 at pin 5.If Vee is fixed, then with proper R10, C_5, and V_{in}, the output signal frequencies (f_0) of LM566 will be I072 Hz and 1272 Hz. The conditions for using LM566 VCO are as follow

$$2k\Omega \leq R_{10} \leq 20k\Omega$$

$$0.75 \leq V_{in} \leq V_{cc}$$

$$f_0 \leq 500 \text{ kHz}$$

$$10\,V \leq V_{cc} \leq 24\,V$$

Figure 13-2 is the circuit diagram of the FSK modulator. The operation theory is to convert the voltage level of the data signal (TTL levels) to the appropriate voltage level. This voltage will be input to the input terminal of LM566 VCO. Ten, the VCO will produce two frequencies with respect to the input voltage levels (1070Hz and 1270Hz). The Q_1, Q_2, R_1, R_3, R_6 VR_1 and VR_2 comprise a voltage converter. In the circuit, Q_1 will operate as NOT gate. When the input signal of the base of Q_1 is high, then Q_1 will switch on. At this moment, the output signal of the collector will be low (around 0.2 V), so Q_2 will switch off. When the input signal of the base of Q_1 is low (0 V), Q_1 will switch off. At this moment, the output signal of the collector of Q_1 is high (5 V), so, Q_2 will switch on. When Q_2 switch off, the input voltage of VCO is

$$V_1 = \frac{VR2}{VR2+R6} Vcc$$

The VCO output signal frequency is f_1. When Q_2 switches on, the inputvoltage of VCO is (assume the resistance of Q_2 is only a few ohm)

$$V2=\frac{VR1/\!/VR2}{(VR1/\!/VR2)+R6}Vcc$$

At this moment, the output signal frequency of VCO is f_2. So, we just need to adjust VR_1 and VR_2, then the output signal frequencies of VCO will become f_1 and f_2 which are 1270 Hz and 1070 Hz, respectively. In figure 13-2, the $U_2, U_3, R_2, R_4, R_5, R_7, R_8, R_9, C_1, C_2, C_3$ and C_4 comprise a 4^{th} order low-pass filter. The objective is to remove the unwanted signal from the LM566 VCO output, so that we can obtain the sinusoidal waveform signal.

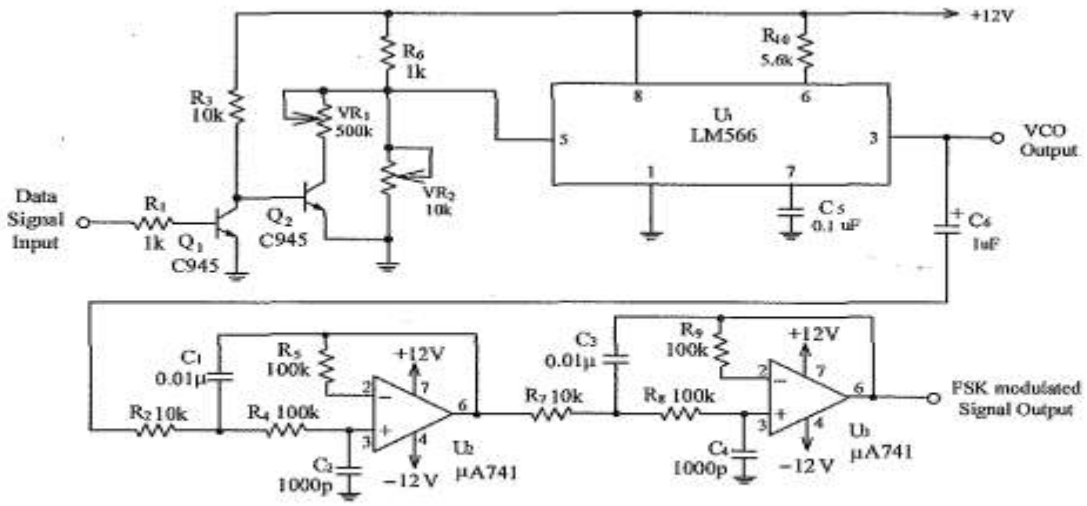


Figure 13-2 The circuit diagram of FSK modulator.

In this experiment, we use the baseband signal as the FSK modulation. If the application is for

wireless transmission, we have to use mixer to convert the signal of baseband to the signal of RF band, then the signal will be able to transmit from antenna. For further RF modulation theory, readers can refer to another book by our company, which is RF Circuit Design.

Experiment Items

Experiment **1:** FSK **modulator**

1. Refer to figure 13-2 or ETEK DA-2000-07 module.
2. At the data signal input terminal (I/P), input 5 V DC voltage, then by using oscilloscope, observe on the output signal frequency ofLM566 at pin 3. Adjust VR_2 carefully so that the frequency of signal generator counter is 870 Hz, and then record the measured results in table 13-1.
3. By using oscilloscope, observe on the output signal of FSK signal output terminal, then record the measured results in table 13-1.
4. At the data signal input terminal (I/P), input 0 V DC voltage (i.e. connect to GND), then by using oscilloscope, observe on the output signal frequency of LM566 at pin 3. Adjust VR_1 carefully so that the output signal frequency of LM566 at pin 3 is 1370 Hz and then recordthe measured results in table 13-1.
5. By using oscilloscope, observe on the output signal of FSK signal output terminal, then record the measured results in table 13-1.
6. Adjust the output voltage of signal generator to TTL level with 200 Hz frequency. Then let this signal input to the data signal input terminal (I/P). By using an oscilloscope, observe on the input signal, the output signal of LM566 at pin 3 arid FSK output terminal signal, then record the

measured results in table 13-2.

7. Adjust the output signal frequency of the signal generator to 5 kHz, the other remains the same. Then let this signal input to the data signal input terminal (1/P). By using an oscilloscope, observe on the input signal, the output signal of LM566 at pin 3 and FSK output terminal signal, then record the measured results in table 13-2.

Measured Results

Table 13-1 The measured results of FSK modulator.

Input Signals	VCO Output Signal WaveformsofLM566 at pin 3	Output Signal Waveforms ofFSK Output Terminal
0v		

5V		

Table 13-2 The measured results of FSK modulator.

Input Signal Frequencies	200Hz	900Hz
Input Signal Waveforms		
VCO Output Signal Waveform of LM566 at pin 3		
FSK Modulated Signal Waveform		

Problems Discussion

1. In figure 13-2, what are the operations of Q_1, Q_2, and LM566?
2. In figure 13-2, what are the operations of VR_1 and VR_2?
3. In figure 13-2, if the input signal is larger than the FSK frequency, will this circuit operate properly? (i.e. compare the 200 Hz and 900 Hz input signals in table 13-2)

Curriculum Objectives

1. To understand the operation theory of FSK demodulator.
2. To implement the FSK detector circuit by using PLL.
3. To understand the operation theory of comparator by usingoperational amplifier as voltage level converter.

Curriculum Theory

In chapter 13 we use-F-SK modulator for k mg distance- communication, which the voltage level of digital signal has been converted to frequency. Therefore, at the receiver, we have to recover the FSK signal to digital signal, that means the frequency should be converted back to voltage. We use phase locked loop (PLL) as FSK demodulator. PLL is a kind of automatic tracking system, which is able to detect the input signal frequency and phase. PLL is widely used in wireless applications, such as AM demodulator, FM demodulator, frequency selector and so on. In the digital

communications, various types of digital PLLs are developed. Digital PLL is very useful in carrier synchronization, bit synchronization and digital demodulation.

PLL can be divided into 3 main parts, which are the phase detector (PD), loop filter (LF) and voltage controlled oscillator (VCO). The block diagram of PLL is shown in figure 14-1.

In chapter 6, we have discussed about the operation theory of PLL. In figure 14-1, when the input signal frequency changes, the output signal ofthe phase detector will change and so as well as the output voltage. We can use this characteristic to design the FSK demodulator. Let the FSK signal frequencies as f1 and f2. Then these signals are inputted to the input terminal of figure 14-1. When the signal frequency is f1, the output voltage will be Vi. When the input signal frequency is f2, the output voltage is V_2. At this moment, we have converted the frequency to voltage. If we add a comparator at the output terminal of PLL, the reference voltage will lie between Vi and V_2, then at the output terminal of comparator, we are able to obtain the digital signal, which is thedemodulated FSK signal.

In this experiment, we implement the FSK demodulator by using LM565 PLL as shown in figure 14-2. The operation frequency of LM565 PLL is below 500 kHz and the internal circuit diagram is shown in figure 14-2. It includes phase detector, voltage controlled oscillator and amplifier. The phase detector is a double-balanced modulator type circuit and the VCO is integrated Schmitt circuit.

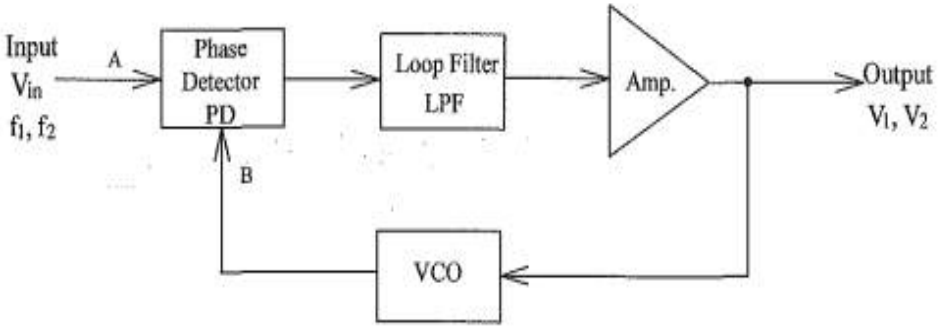


Figure 14-1 The block diagram of PLL.

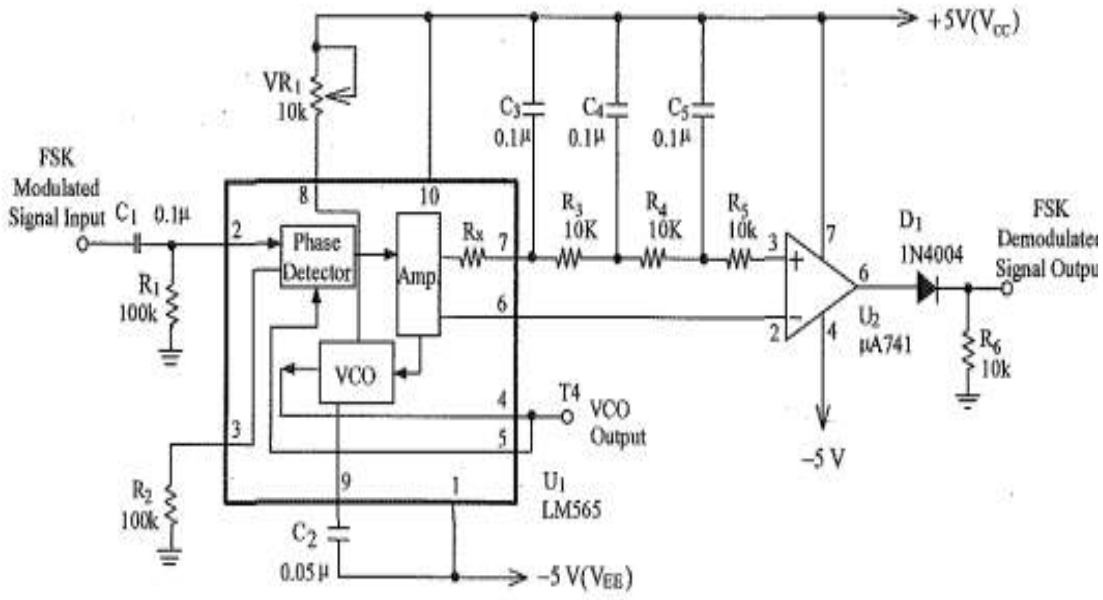


Figure 14-2 The internal circuit diagram of FSK demodulator.

Pin I is connected to negative voltage supply, VEE • Pins 2 and 3 are connected to the input signals, but normally pin 3 will connect to ground. If pins 4 and 5 are connected to frequency multiplier, then various multiplications of frequencies can be obtained. In this

experiment, we need not use the frequency multiplier, therefore, these two pins are shorted. **Pin** 6 is the reference voltage output. The internal resistor (R_x) of pin 7 and the external capacitor (C_3) comprise a loop filter. Pin 8 is connected to timing resistor (VR_1). Pin 9 is connected to a timing capacitor (C_2) . Pin 10 the positive voltage supply (V_{cc}) of LM565. The important parameters of LM565 PLL circuit design are as below

1. The Free-Running Frequency ofLM565

When LM565 without any input signal, the output signal of VCO is called free-running frequency. The C_2 is timing capacitor and the variable resistor VR_1 is timing resistor. The free-running frequency (f_0) of VCO of the LM565 is determined by C_2 and VR_1. The expression is

$$f_0 \approx \frac{1.2}{4 VR_1 C_2} \qquad (14\text{-}1)$$

2. The Locked Range ofLM565

When the PLL is in locked conditions, if the frequency of the input signal (f_i) deviates from f_0 , then the PLL will remain in the locked condition. When f_i reaches a certain frequency, which the PLL is not able to lock, then the difference between f, and f_0 is called the locked range.

The locked range ofLM565 can be expressed as

$$f_L = \frac{8 f_o}{V_c} = \frac{8 f_o}{V_{cc} - V_{EE}} \qquad (14\text{-}2)$$

3. The Captured Range ofLM565

The initial mode of PLL is in unlocked condition, then the frequency of the input signal (f,)

will come near to f_0 • When f_i reaches a certain frequency, the PLL will be in locked condition. At this moment, the difference between f_i and f_0 is called the captured range. The captured range ofLM565 can be expressed as

$$f_C = \frac{1}{2\pi}\sqrt{\frac{2\pi \times f_L}{3.6\times10^3 \times C_2}} \qquad (14\text{-}3)$$

In figure 14-2, pin 7 of LM565 is connected to R_3, R_4, R_5, C_3, C_4 and C_5 to comprise-a low-pass filter. The objective is to remove the unwanted signal, which will cause the comparator produce incorrect action. U_2 is the comparator and its reference voltage is inputted at pin 6 of LM565. The output voltage of LM565 will pass through U_2 and D_1 to obtain the output voltage of digital signal of TTL level.

Experiment Items

Experiment 1: FSK demodulator

1. In figure 14-2 or ETEK DA-2000-07 module. Without adding any signal at the input terminal, then by using an oscilloscope, observe the VCO output (T_1) of LM565, adjust VR1 so that the free-running frequency of LM565 operates at 1170 Hz.
2. At the input terminal (1/P), input 870 Hz frequency and 8 $\mathbf{V_{PP}}$ sine wave amplitude. By using an oscilloscope and switching to DC channel, then observe on the output signal waveform and record the measured results intable 14-1.
3. At the input terminal, input 1370 Hz sine wave frequency and 8 VPP amplitude. By using an oscilloscope and switching to DC channel, then observe on the output signal waveform and record the measured results in table 14-1.
4. Using figure 13-2 FSK modulator in chapter 13 as the signal source, thenat the input terminal of the FSK modulator in figure 13-2, input 150 Hz frequency and square wave in TTL level.
5. Let the output signal of the FSK modulator in figure 13-2 connects to the input terminal of the

FSK demodulator in figure 14-2. By using an oscilloscope and switching to DC channel, then observe on the output signal waveform and record the measured results in table 14-2 (if unable to get the demodulated signal, you may need to check the FSKsignal input whether operate at 870 Hz or 1370 Hz).

6. Let the input signal frequency of the input terminal of the FSK modulatorin figure 13-2 be 200 Hz, the others remain the same. By using oscilloscope and switching to DC channel, then observe on the output signal waveform and record the measured results in table 14-2.

Measured Results

Table 14-1 The measured results of the FSK demodulator (Vin = 8 VPP).

Input Carrier Signal Frequencies	Input Carrier Signal Waveforms	FSK Demodulated Signal Waveforms
870Hz		

1370 Hz		

Table 14-2 The measured results of FSK demodulator.

Input Data Signal Frequencies	FSK Modulated Signal Waveforms	FSK Demodulated SignalWaveforms
150 Hz		
200Hz		

Problems Discussion:

I. In figure 14-2, what are the factors that determine the free-runningfrequency ofLM565 PLL?

2. In figure 14-2, what are the purposes ofμA741?

3. In figure 14-2, what are the functions of pin 6 ofLM565?

4. Why the output signal of LM565 must pass through the multi-stageslow-pass filter, and then connects to the comparator?

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Optical Fiber Communication Lab Manual

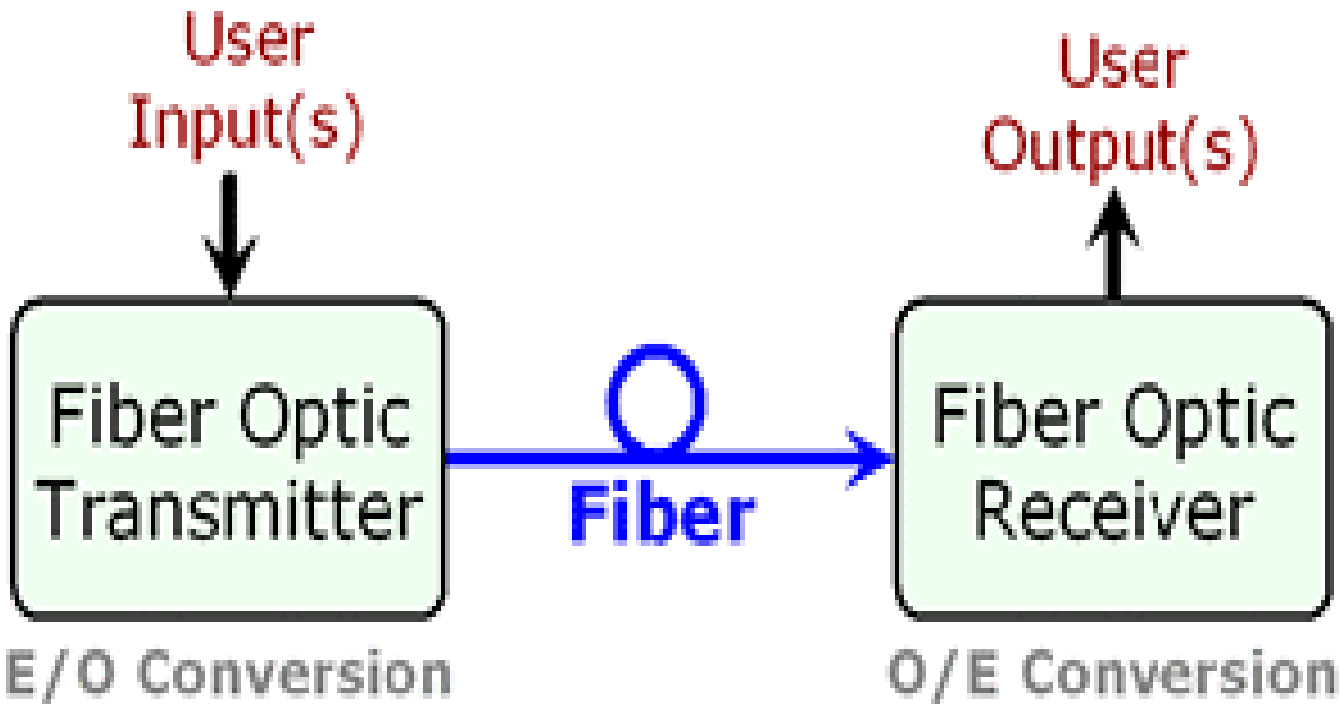
What is optical fiber communication?

Fiber-optic communication

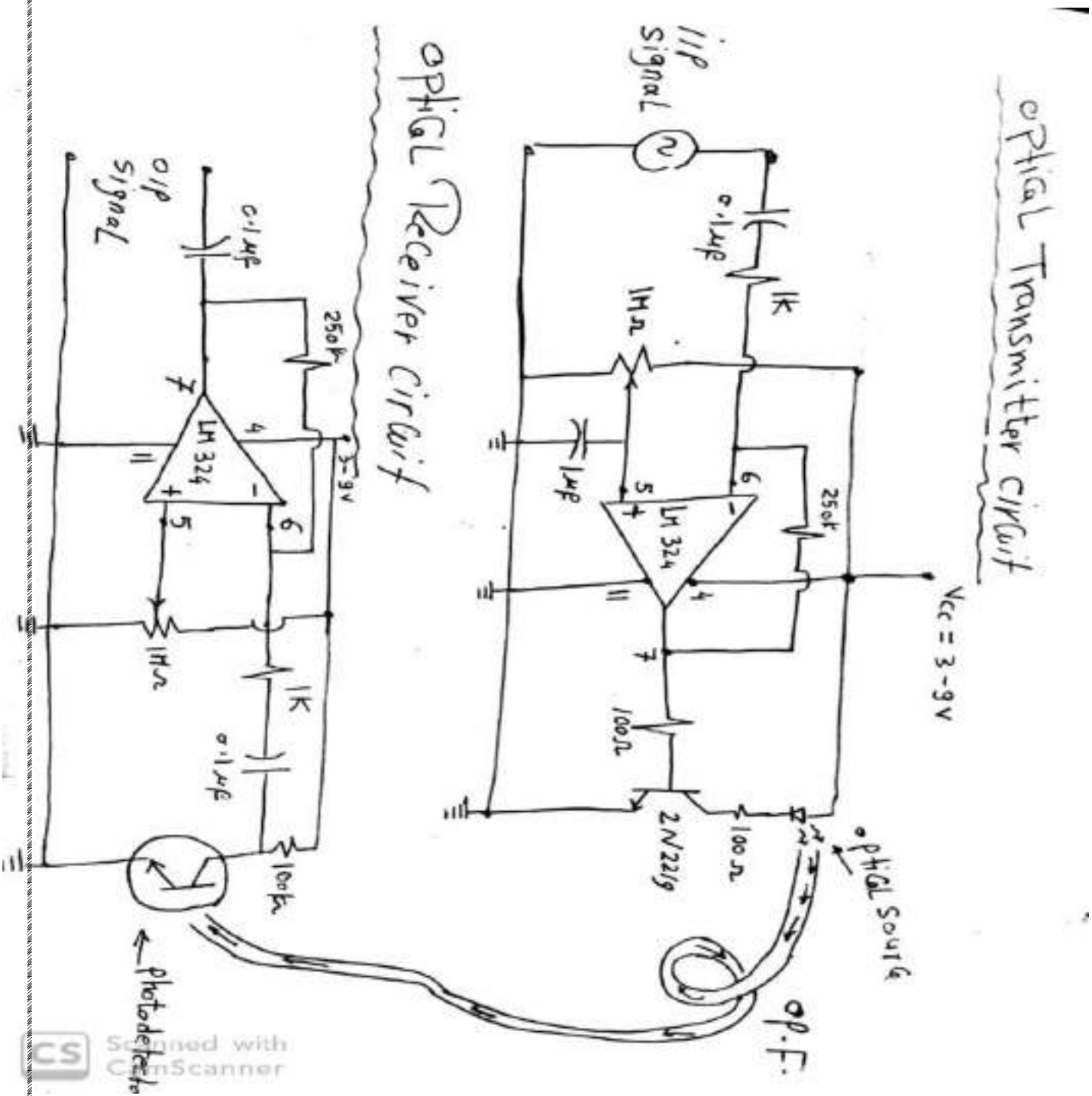
is a method of transmitting information from one place to another by sending pulses of infrared light through an optical fiber. The light is a form of carrier wave that is modulated to carry information.

The Fiber Optic data Communication System Include :-

- **Fiber optic Transmitter**
- **Fiber link**
- **Fiber optic Receiver**



Optical Fiber Communication System Block Diagram.



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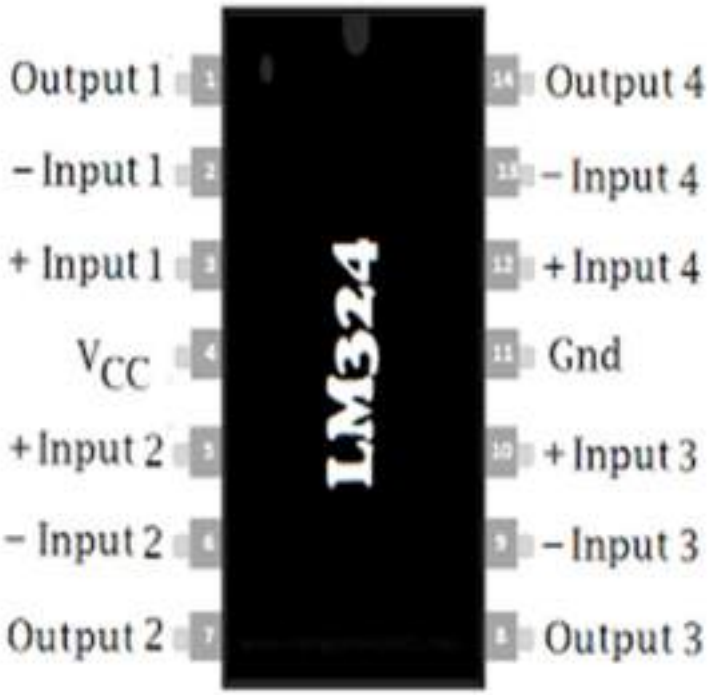
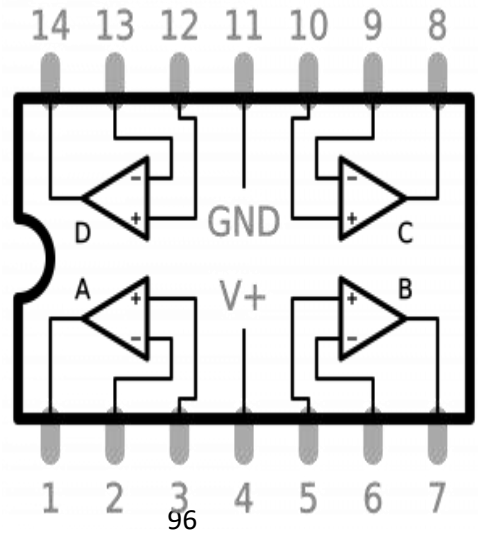
Optical Fiber Component Datasheet

1) Lm324 Datasheet

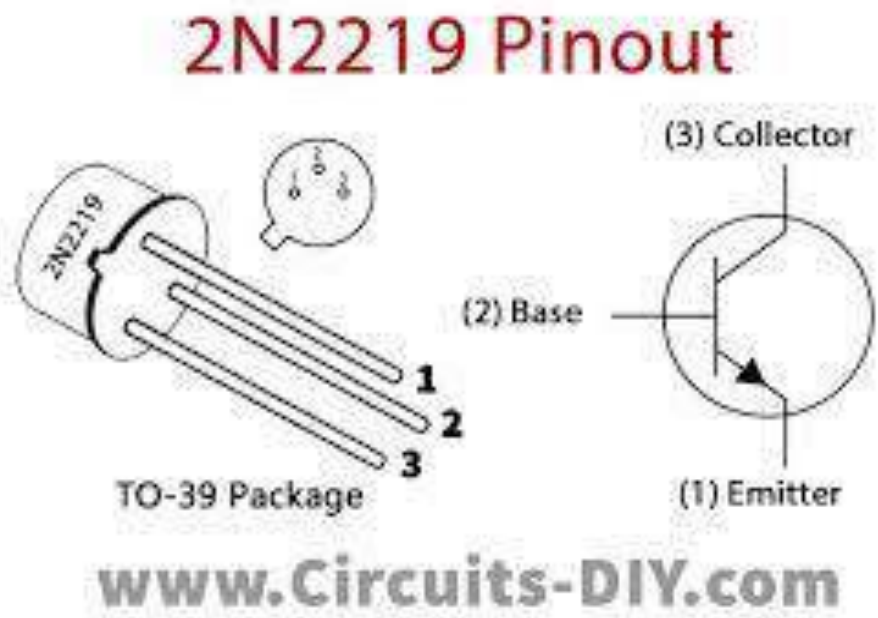
- **The LM324 IC consists of 14-pins with four independent op-amps in one package.**





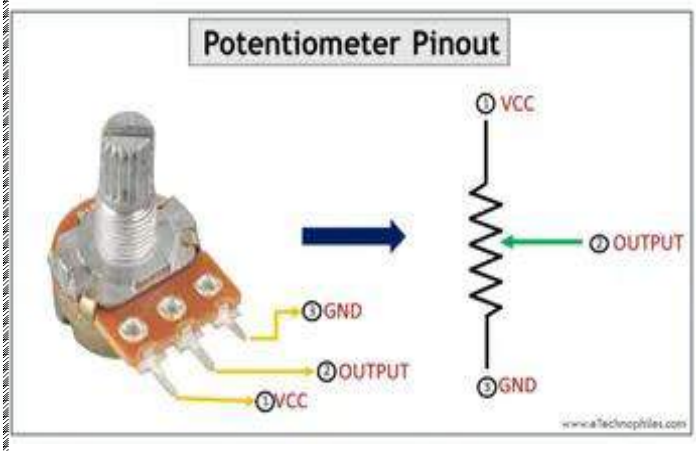
2) 2N2219 Datasheet.

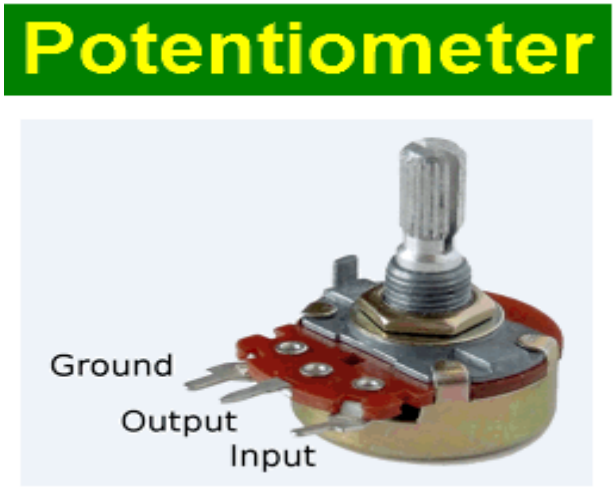
- **2N2219 is a NPN transistor**



3) A Potentiometer.

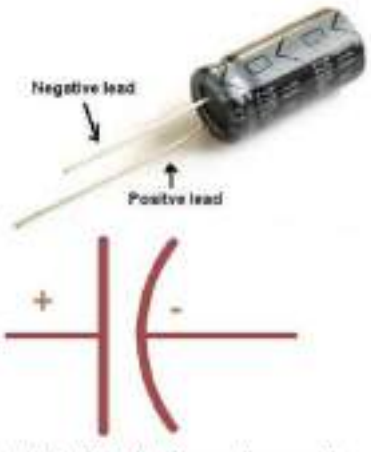
- **is a three-terminal resistor with a sliding or rotating contact that forms an adjustable voltage divider.**





4) Capacitor Datasheet

- **The Electrolytic Capacitors have polarity. Meaning they have a positive and negative pin. The pin which is long is the positive pin and the pin which is short is the negative pin.**



Polarized Electrolytic Capacitor and its electric Symbol

Non-Polarized Ceramic Capacitor and its electric Symbol

5)Resistor Datasheet

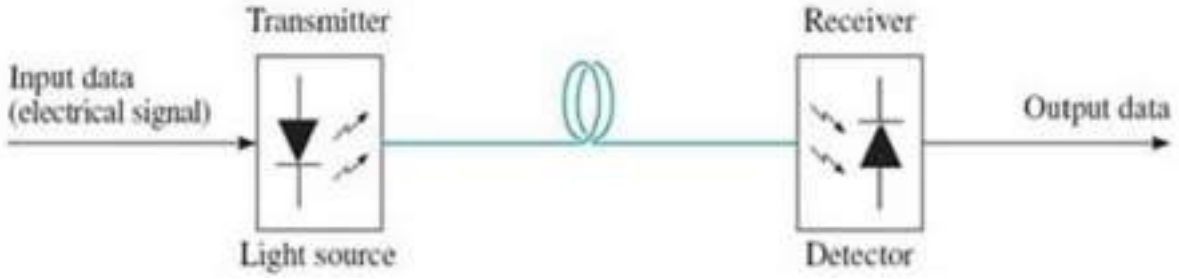
- **A resistor is a two-terminal electrical component that opposes the passage of an electric current.**
- **Resistor reduces current flow, adjusts signal levels, divides voltages, and terminates transmission lines.**

6) Optical Source.

- **Optical transmitter coverts electrical input signal into corresponding optical signal.**
- **The optical signal is then launched into the fiber.**
- **Popularly used optical transmitters are Light Emitting Diode (LED) and semiconductor Laser Diodes (LD).**

7) Optical Detector.

- **The photo detector works on the principle of optical absorption.**
- **The main requirement of light detector is its fast response.**
- **For fiber optic communication purpose most suited photo detectors are PIN (p-type-Intrinsic-n-type) diodes and APD (Avalanche photodiodes).**


Transmitter
Receiver
Input data
(electrical signal)
Output data
Light source
Detector

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Analog Communication System
Lab Manual

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AM Modulation

1. To understand the basic theory of amplitude modulation.
2. To understand the waveform and frequency spectrum of amplitude modulation, also calculate the percentage of modulation.
3. To design and implement the amplitude modulator.
4. To understand the measurement and adjustment of amplitude modulation circuit.

Curriculum Theory

In amplitude modulation (AM), we utilize the amplitude of audio signal to modulate the amplitude of carrier signal, which means that the amplitude of carrier signal will be varied with amplitude of audio signal. The waveform is shown in Figure 3-1. Let the audio signal be $A_m COS(2\pi f_m t)$ and carrier signal be $A_C COS(2\pi f_m t)$, then the amplitude modulation can be expressed as

$$x_{AM}(t) = [A_{DC} + A_m \cos(2\pi f_m t)] A_c \cos(2\pi f_c t) = A_{DC} A_c [1 + m\cos(2\pi f_m t)] \cos(2\pi f_c t) \quad (3\text{-}1)$$

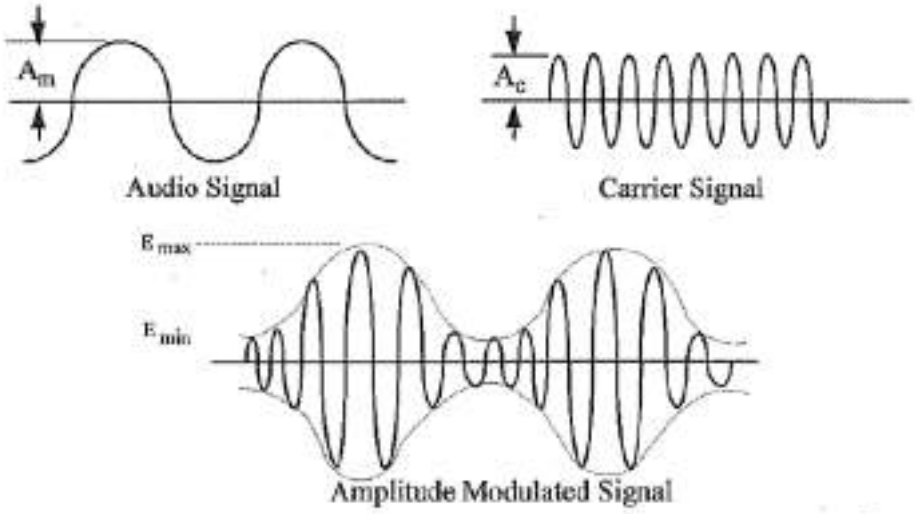

Figure 3-1 Signal waveform of amplitude modulation.

Where

$$m = A_m / A_{DC}$$

A_{DC} : DC signal magnitude.

A_m : Audio signal amplitude. A_C : Carrier signal amplitude. F_m : Audio signal frequency. F_C : Carrier signal frequency.

m: Modulation index or depth of modulation.

We can rewrite equation (3-1) as

$$x_{AM}(t) = \frac{1}{2} A_{DC} A_c m \{\cos[2\pi(f_c - f_m)t] + \cos[2\pi(f_c + f_m)t]\}$$

$$+A_{DC} Ac \cos(2\pi f_C t) \qquad (3\text{-}2)$$

The first term represents double sideband signals; the second term represents carrier signal. From equation (3-2), we can sketch the frequency spectrum of amplitude modulation as shown in figure 3-2. Since the audio signal is hidden in the double sidebands and the carrier signal does not contain any message, therefore the power is consumed in carrier during transmission of amplitude modulation signal. For this reason, the transmission-efficiency of AM modulation is lower than double sidebands suppressed carrier (DSB-SC) modulation but its demodulation circuit is much simpler.

There is an important parameter "m" in equation (3-1) called modulation index or depth of modulation. Normally it is represented in percentage, so we also call modulation percentage. The definition is as follow:

$$m = \frac{\text{Audio signal amplitudex}}{DC\ signal\ magnitude} \times 100\% = \frac{A_m}{A_{DC}} \times 100\% \qquad (3-3)$$

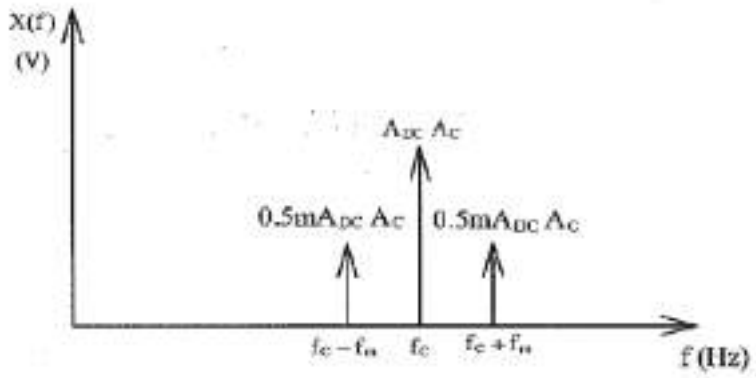

Figure 3-2 Frequency spectrum of amplitude modulation signal.

Generally, the magnitude of DC signal is not easy to measure; therefore we express the modulation index in another form

$$m = \frac{E_{max} - E_{min}}{E_{max} + E_{min}} \times 100\ \% \qquad (3\text{-}4)$$

Where E_{max} and E_{min} as shown m Figure 3-1 are $E_{max} = A_c + A_m$ and $E_{min} = A_c - A_m$.

We know that at amplitude modulation, the audio signal is hidden in the double sidebands, so if the double sideband signals are getting stronger, the transmission efficiency is getting better. From equation (3-2), we know that the double sideband signals are proportional to the modulation index. Thus the larger the modulation index, the better the transmission efficiency. Normally modulation index is smaller or equal to 1. If greater than 1, we call it over modulation.

In this experiment, we utilize the balanced modulator MCI496 to implement amplitude modulator. Follow the variation of input signal frequency, the balanced modulator (MC1496) can become a frequency multiplier, amplitude modulator or double sidebands suppressed carrier modulator (DSB-SC Modulator). Its input signal, output signal and circuit characteristics are shown in Table 3-1.

Figure 3-3 is the internal circuit ofMC1496, where D_1, R_1, R_2, R_3, Q_7 and Q_8 comprise an electric current source, which can supply DC bias current for Q_5 and Q_6. Q_5 and Q_6 comprise a differential combination to drive the dual differential amplifiers constructed by Q_1, Q_2, Q_3 and Q_4. Pin 1 and 4 are the inputs of audio signal; Pin 8 and 10 are the inputs of carrier

Signal

Table 3-1 Three different types of modulation signal produced by different signals frequency of balanced modulator.

Input Carrier Signal	Input Audio Signal	Output Balanced Modulator	Circuit Characteristics
f_c	f_c	$2f_c$	Frequency Multiplier
f_c	f_m	f_c, $f_c + f_m$, $f_c - f_m$	Amplitude Modulator
f_c	f_m	$f_c + f_m$, $f_c - f_m$	DSB-SC Modulator

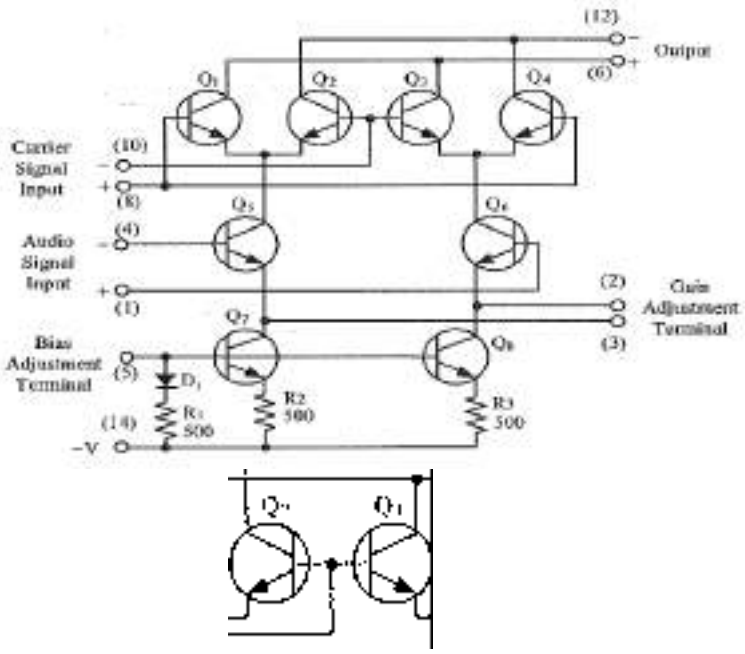

Figure 3-3 The internal circuit of MCI 496.

The resistor between pins 2 and 3 controls the gain of the balanced modulator; the resistor of pin 5 determines the magnitude of bias current for amplifier.

Figure 3-4 is the circuit diagram of amplitude modulation. We can see that the carrier signal and audio signal belong to single ended input. Thecarrier signal input from pin 10 and the audio signal input from pin 1.

Therefore R_8 determine the gain of the whole circuit and R_9 determine the magnitude of bias current. If we adjust the variable resistor VR1 or change the input amplitude of audio signal, then we can control the percentage modulation of amplitude modulation.

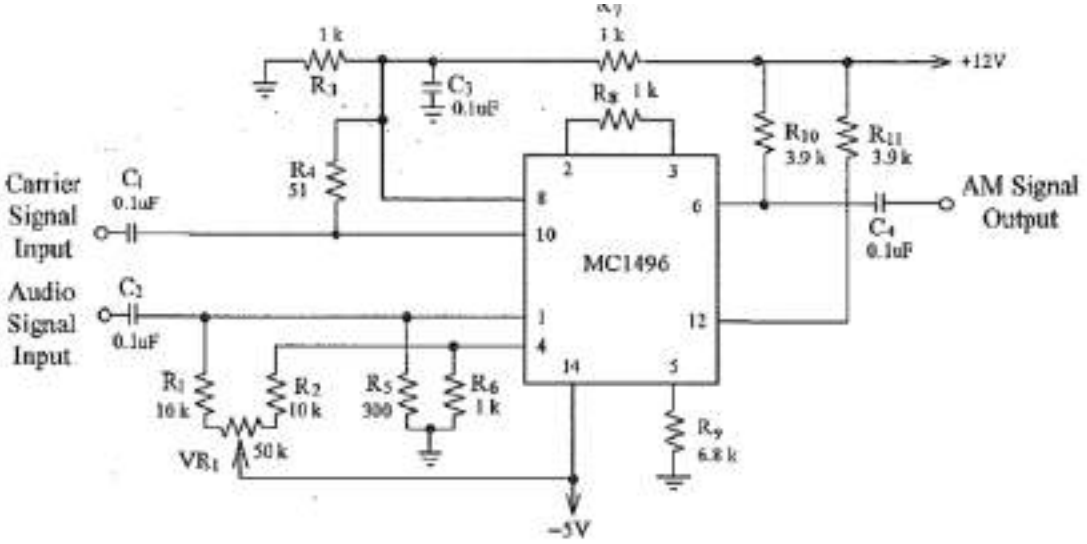

Figure 3-4 Circuit diagram of amplitude modulation by utilizing MCI 496.

Experiment Items

Experiment 1: Amplitude modulator

1. Refer to figure 3-4 or ETEK DA-2000-02 module, let J1 and J3 short circuit, J2 and J4 be open circuit; i.e. $R_8 = 1\ k\Omega$ and $R_9 = 6.8\ k\Omega$.

2. At audio signal input port (I/ P2), input 1.2 Vpp amplitude, 1 kHz sine wave frequency; at carrier signal input port (I/ Pl), input 1.2 Vpp amplitude, 500 kHz sine wave frequency.

3. By using oscilloscope, observe on output signal waveform at amplitude modulation signal output port (o/P). Adjust VR_1, until the modulation percentage reach 50 %, records the measured results of output signal waveform in table 3-2

4. By using spectrum analyzer to observe the frequency spectrum ofoutput signal and record the measured results in table 3-2.

5. Substitute the measurement results into equation (3-4), find the modulation percentage and record in table 3-2.

6. Change the amplitude of audio signals to 1 V_{PP} and 800 mV_{PP}. The others remain the same. Observe on output signal waveform and record the measured results in table 3-2.

7. Repeats steps 4 and 5.

8. At audio signal input port (I/ P2), input 1 v_{pp} amplitude, 1 kHz sine wave frequency; at carrier signal input port (I/ Pl), input 400 mV_{pp} amplitude, 500 kHz sine wave frequency.

9. By using oscilloscope, observe on output signal waveform at amplitude modulation signal

10. output port (O / P) and record the measured results in table 3-3.

11. By using spectrum analyzer, observe on the frequency spectrum of output signal and record the measured results in table 3-3.

12. Substitute the measured results into equation (3-4), find the modulation percentage and record measured results in table 3-3.

13. Change the amplitude of audio signals to 600 mV_{PP} and 800 mV_{PP}. The others remain the same. Repeat steps 9, 10 and 11.

14. At audio signal input port (I/ P2), input 800 mV_{PP} amplitude, 2 kHz sine wave frequency; at carrier signal input port (I/ Pl), input 1 V_{pp} amplitude, 500 kHz sine wave frequency.

15. By using oscilloscope, observe on the output signal waveform at amplitude modulation signal output port (O/P) and record the measured results in table 3-4.

16. By using spectrum analyzer, observe on the frequency spectrum of output signal and record the measured results in table 3-4.

17. Substitute the measured results into equation (3-4), find the modulation percentage and record the measured results in table 3-4.

18. Change the frequencies of audio signal to 1 kHz and 900 Hz. The others remain the same. Repeat steps 14, 15 and 16.

19. At audio signal input port (I/P2), input 800 mV_{PP} amplitude, 2 kHz sine wave frequency; at carrier signal input port (I/Pl), input 1 V_{pp} amplitude, 500 kHz sine wave frequency.

20. By using oscilloscope, observe on the output signal waveform at amplitude modulation signal output port (O/P) and record the measuredresults in table 3-5.

21. By using spectrum analyzer, observe on the frequency spectrum ofoutput signal and record the measured results in table 3-5.

22. Substitute the measured results into equation (3-4), find the modulationpercentage and record the measured results in table 3-5.

23. Change the frequencies of carrier signal to 800 kHz and 1 MHz. Theothers remain the same. Repeat steps 19, 20 and 21.

Measured Results

Table 3-2 Observe on the variation of amplitude modulation by changing theamplitude of audio signal (Vc=1.2Vpp, fc= 500 kHz, f_m = 1 kHz).

Audio Signal Amplitude	Output Signal Waveform	Output Signal Frequency Spectrum	Modulation Percentage
1.2 V_{pp}	E_{max} = **Emin** =		-
1 V_{pp}	E_{max} = **Emin** =		
800 mV_{pp}	E_{max} = **Emin** =		

Table 3-3 Observe on the variation of amplitude modulation by changing theamplitude of carrier signal (W_m = 1 V_{pp}, fc = 500 kHz, f_m = 1 kHz),

Carrier Signal Amplitude	Output Signal Waveform	Output Signal Frequency Spectrum	Modulation Percentage
400 mV_{pp}	E_{max} = **Emin** =		
600 mV_{pp}	E_{max} = **Emin** =		
800 mV_{pp}	E_{max} = **Emin** =		

Table 3-4 Observe on the variation of amplitude modulation by changing thefrequency of audio signal (V, =1 V_{pp}, Vm =800 mV_{pp} fc=500 kHz).

Audio Signal Frequency	Output Signal Waveform	Output Signal Frequency Spectrum	Modulation Percentage
2kHz	E_{max} = **Emin** = .		
1 kHz	E_{max} = **Emin** =		
900Hz	E_{max} = **Emin** =		

Table 3-5 Observe on the variation of amplitude modulation by changing thefrequency of carrier signal (V= 1 Vpp , V_m= 800 mVPP , fm = 2 kHz).

Carrier Signal Frequency	Output Signal Waveform	Output Signal Frequency Spectrum	Modulation Percentage
500kHz	E_{max} = **Emin** =		
S00kHz	E_{max} = **Emin** =		
I MHz	E_{max} = **Emin** =		

Problems Discussion

1. From figure 3-4, if we change the value of resistor R_8, then what will happen for the output signal of amplitude modulator? Let J2 be short circuit, JI be open circuit, i.e. R_8 changes to R_{12}, its values is 1 kΩ to 2kΩ, then what will happen for the output signal of amplitude modulator?

2. From figure 3-4, if we change the value of resistor R_9, then what will happen for the DC bias current ofMC1496? Let J4 be short circuit, J3 be open circuit, i.e. R_9 changes to R_{13}, its values is 6.8 kΩ to 10 kΩ, then what will happen for the DC bias current of MC1496?

3. When modulation percentage, m = 50 %, what is the ratio of E_{max} and E_{min}?

4. Try to explain the motivation of objectives of variable resistor VR_1•

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AM DEMODULATION

Curriculum Objectives –

1. To understand the theory of amplitude demodulation.
2. To design and implement the diode detection amplitudedemodulation.
3. To design and implement the product detection amplitudedemodulator.

Curriculum Theory:

From Chapter 3, we know that the amplitude modulation signal utilizes the amplitude of audio signal to modulate high frequency carrier signal. Therefore, when we receive the amplitude modulation signal, we need to restore the audio signal. Figure 4-1 is the theory diagram of amplitude modulation. Normally detector can be classified as synchronous detector and asynchronous detector. We will discuss these two types of detectors in this chapter.

1. Diode Detector for Amplitude Demodulation

Since amplitude modulation signal utilizes audio signal to modulate carrier signal, which means the variation of carrier signal amplitude is followed by the change of audio signal amplitude. Hence the objective of amplitude demodulator is to take out the variation envelop detection from amplitude modulation signal.

Figure 4-2 is the block diagram of rectification demodulator. This circuit is a typical asynchronous detector. It rectifies the amplitude modulation signal and obtains a positive half wave signal. After that the signal will pass through a low-pass filter and obtain an envelop detection. Then get rid of the DC signal, the audio signal will be recurred.

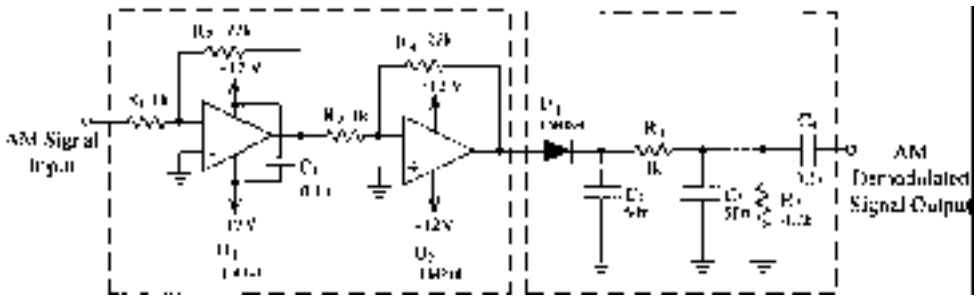

Figure 4-3 The circuit diagram of diode detector.

Figure 4-3 is the circuit diagram of diode detector, in which R_1, R_2, R_3, R_4, U_1 and U_2 form two groups of inverting amplifiers to amplify the input signal; D_1 is the rectifier diode which can make the amplitude modulation signal become a positive half wave signal; C_2, C_3 and R_5 comprise a low-pass filter to remove the envelop detection signal of audio signal which includes the DC level; then finally the objective of C_4 is to block the DC level and we can obtain a pure audio signal at output port.

2. Product Detector for Amplitude Demodulation

The amplitude demodulator can be implemented by utilizing a balanced modulator. We call this type of modulator as synchronous detector or product detector. Figure 4-4 is the internal structure circuit diagram of MC1496 balanced modulator (refer to chapter 3 for the circuit description). Let $X_{AM}(t)$ be the amplitude modulated signal, $x_c(t)$ be the carrier signal,

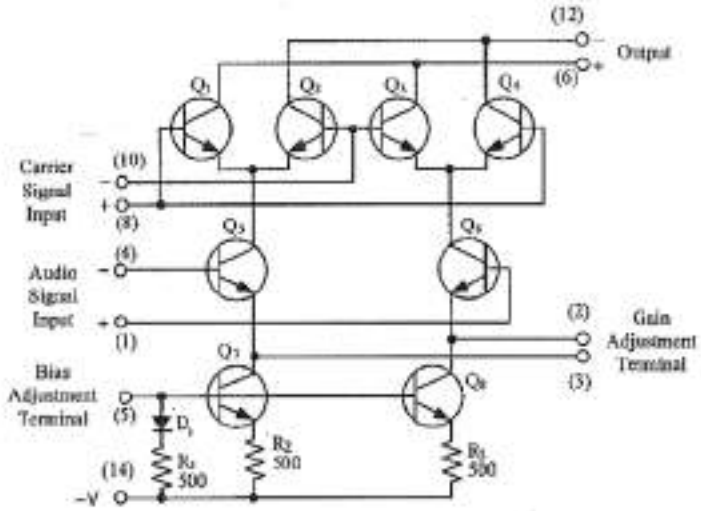

Figure 4-4 MC 1496 internal structure circuit diagram.

$$x_{AM}(t) = A_{DC}\left[1 + m\cos(2\pi f_m t)\right]\left[A_c \cos(2\pi f_c t)\right] \quad (4\text{-}1)$$

$$x_c(t) = A_c\cos(2\pi f_c t) \quad (4\text{-}2)$$

When these two signals input into two differential ports of balanced modulator, then the balanced modulator output signal is as follow

$$X_{out} = kX_c(t)X_{AM}(t)$$

$$= kA_{DC}A^2{}_c[1 + m\cos(2\pi f_m t)\cos^2(2\pi f_c t)]$$

$$= \frac{kA_{DC}A^2{}_c}{2} + \frac{kA_{DC}A^2{}_c}{2} m\cos(2\pi f_m t)$$

$$+ \frac{kA_{DC}A^2{}_c}{2}[1 + m\cos(2\pi f_m t)\cos(2\pi f_c t)] \quad (4-3)$$

Where k represents the gain of the balanced modulator. The first termis the DC signal, second term is the audio signal and third term is the second

harmonic of amplitude modulated signal. If we can take out the second term from Xout (t), then we can obtain the exact amplitude demodulated signal or audio signal.

Figure 4-5 is the circuit diagram of product detector. VR_1 controls theinput magnitude of carrier signal; VR_2 controls the input magnitude of amplitude modulated signal; then the output signal of MC1496 is located

at pin 12. C_1, c_9. and R_9. comprise a low-pass filter which can remove the unwanted third term of equation (4-3), i.e. second harmonic of amplitude modulated signal. The DC signal, which is the first term of equation (4-3), can be blocked by C_{10}• Therefore the signal that we obtain at output port will be:

$$X_{out}(t) = \frac{kA_{DC}A^2_c}{2} mcos(2\pi f_m t) \qquad (4\text{-}4)$$

Equation (4-4) represents the audio signal or in other words the original amplitude modulated signal can be taken out via product detector.

These two types of detectors have its own advantages and disadvantages. As for diode detector, which is asynchronous detector, its circuit is simple but the performances are not as better as product detector. However for product detector, which is synchronous detector, it has good performances but the circuit is more complicated than diode detector.

Further more it also requires synchronous for both earner signal and amplitude modulated signal (same frequency and same phase), otherwise it will affect the quality of the output signal.

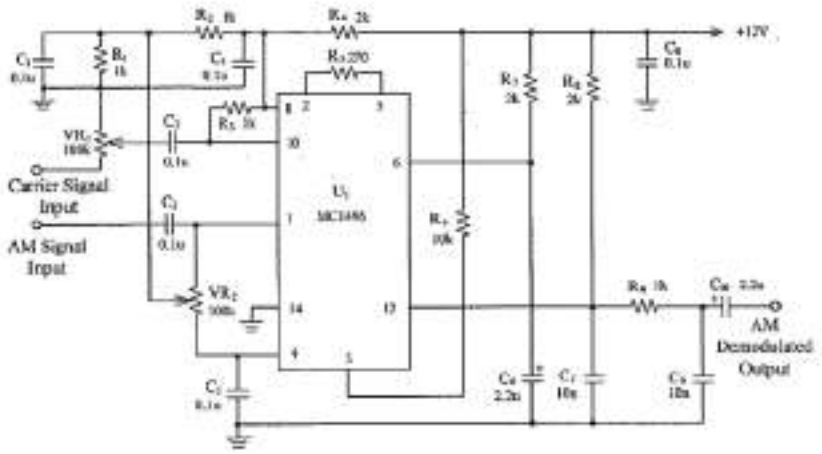

Figure 4-5 The circuit diagram of product detector.

Experiment Items

Experiment 1: Diode detector of amplitude demodulator

1. Utilize the amplitude modulator in chapter 3 (as shown in figure 3-4) or refer to ETEK DA-2000-02 module, produce an amplitude modulated signal as the amplitude modulated signal source in this experiment.

2. Let J2 and J4 be short circuit.

3. From the input amplitude modulator, adjust the amplitude and frequency of the carrier signal be 600 mV_{pp} and 300 kHz sine wave, and also adjust the amplitude and frequency of audio signal be 600mV_{pp} and 2 kHz sine wave.

4. By using oscilloscope, observe on the output waveform of amplitude modulator, then adjust VR_1 of the amplitude modulator until the modulation percentage reaches 100 %.

5. Connect the output signal of the amplitude modulator to the input port(I/ P) of diode detector in figure 4-3 or ETEK DA-2000-02 module.

6. By using oscilloscope, observe on the amplified signal waveform and output waveform of diode detection, then record the measured results in table 4-1

7. Change the frequencies of audio signal to 1 kHz and 900 Hz, the others remain the same, and then repeat step 6. and 2 kHz sine wave.

8. By using oscilloscope, observe on the output waveform of amplitude modulator, then adjust VR_1 of the amplitude modulator until the modulation percentage reaches I00 %.

I0. By using oscilloscope, observe on the amplified signal waveform and output waveform of diode detection, then record the measured results in table 4-2.

11. Change the frequencies of audio signal to 1 kHz and 900 Hz, the others remain the same, and then repeat step 10.

Experiment 2: Product detector of amplitude demodulator

1. Utilize the amplitude modulator in chapter 3 (as shown in figure 3-4) or refer to ETEK DA-2000-02 module, produce an amplitude modulated signal as the amplitude modulated signal source in this experiment.
2. Let J2 and J4 be short circuit.
3. From the input amplitude modulator, adjust the amplitude and frequency of the carrier signal be 600 mV_{PP} and 500 kHz sine wave, and also adjust the amplitude and frequency of audio signal be 600 mV_{PP} and 2 kHz sine wave.
4. By using oscilloscope, observe on the output waveform of amplitude modulator, then adjust VR_1 of the amplitude modulator until the modulation percentage reaches 100 %.
5. Connect the output signal of the amplitude modulator to the input port (I/ P2) of product detector in figure 4-5 or ETEK DA-2000-02 module. At the same time, connect the same carrier signal from amplitude modulator to the carrier input port (I /Pl) of product detector.
6. By using oscilloscope, observe on the output waveform of product detection, then record the measured results in table 4-3.
7. Change the frequencies of audio signal to 1 kHz and 900 Hz, the others remain the same, and then repeat step 6.
8. From input amplitude modulator, adjust the amplitude and frequency of carrier signal be 600 mV_{PP} and 500 kHz sine wave, and also adjust the amplitude and frequency of audio signal be 600 mV_{PP} and 2 kHz sine wave.
9. By using oscilloscope, observe on the output waveform of amplitude modulator, then adjust VR_1 of the amplitude modulator until the modulation percentage reaches 100 %.

10. By using oscilloscope, observe on the output waveform of product detection, then record the measured results in table 4-4.

11. Change the frequencies of audio signal to 800 kHz and 1 MHz, the others remain the same, and then repeat step 10.

Measured Results

Table 4-1 The measured results of diode detector of amplitude demodulator(V_C= 600 mV_{pp}, V_m = 600 mV_{pp}, f_C=300 kHz).

Audio Signal Frequencies	Input signal Waveforms	Detector Output Signal Waveforms
2kHz		
1 kHz		
900Hz		

Table 4-2 The measured results of diode detector of amplitude demodulator (V_C= 300 mV_{pp}, V_m = 600 mV_{pp}, f_C=300 kHz).

Audio Signal Frequencies	Input Signal Waveforms	Detector Output Signal Waveforms
2kHz		
1 kHz		
900Hz		

Table 4-3 The measured results of product detector of amplitude demodulator(V_C= 600 mV_{pp}, V_m = 600 mV_{pp}, f_C=500 kHz, m=100%).

Audio Signal Frequencies	Input Signal Waveforms	Detector Output Signal Waveforms
2kHz		
1 kHz		
900Hz		

Table 4-4 The measured results of product detector of amplitude demodulator (V_C= 600 mV_{pp}, V_m = 600 mV_{pp}, f_C=2kHz, m=100%).

Carrier Signal Frequencies	Input Signal Waveforms	Detector Output Signal Waveforms
500 kHz		
800kHz		
1MHz		

Problems Discussion

1. In figure 4-3, if we connect the output of amplitude modulator to diode detector without the µA741 operation amplifier, what will the results be?

2. In figure 4-5, if the carrier signal and amplitude modulated signal are asynchronous, then what will the results be?

3. In figure 4-5, what are the objectives of R_9, C_7 and C_9?

4. In figure 4-5, what are the objectives of VR_1 and VR_2?

5. In figure 4-5, what are the objectives of R_5 and R_6?

Ministry of Higher Education
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Communications and Electronics Department

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FM MODULATION

Curriculum Objectives

1. To understand the characteristics of varactor diodes.
2. To understand the operation theory of voltage controlledoscillator (VCO).
3. To design and implement the voltage controlled oscillator andfrequency modulator.

Curriculum Theory

1. The Operation Theory of FM Modulation In frequency modulation (FM), we utilize the amplitude of audio signal to modulate the frequency of carrier signal. The transmitted high and low frequency signals will follow the received audio signal, which has different frequency that keeps on changing. The frequency modulation can be expressed as

$$x_{FM}(t) = A_c \cos \theta(t) = A_c \cos [2\pi f_c t + 2\pi f_\Delta \int x(\lambda)\, d\lambda] \qquad (5\text{-}1)$$

Then

$$x_{FM}(t) = A_c \cos\left[2\pi f_c t + \frac{f_\Delta A_m}{f_m} \sin(2\pi f_m t)\right]$$

Where= $A_c \cos[2\pi f_c t + \beta \sin(2\pi f_m t)]$

$\theta(t)$: Instantaneous modulated frequency.F_c: Carrier frequency.

f_m : Modulating frequency or audio signal frequency

β : Modulation index, $\beta = A_m (f_\Delta / f_m)$.

f_Δ: Frequency-deviation.

Frequency deviation of FM $X_{FM}(t)$ is shown as below

$$f = \frac{1}{2\pi}\frac{d}{dt}\theta(t) = \frac{1}{2\pi}\frac{d}{dt}[2\pi f_c t + \beta \sin(2\pi f_m t = f_c + f_\Delta \cos(2\pi f_m t) = f_c + \Delta_m \cdot f_\Delta \cdot \cos(2\pi f_m t)$$

(5-3)

From equation (5-3), we know that when the amplitude of modulating signal changes, the frequency of FM will change too, and it uses the center point of carrier frequency to achieve frequency deviation. From Carson's rule, the bandwidth (BW) of modulated signal can be expressed as

$$BW = 2(\beta + 2) \cdot f_m = 2\left\{\frac{A_m \cdot f_\Delta}{f_m} - 2\right\} \cdot f_m = 2(A_m f_\Delta + 2f_m)$$

If the FM signal is the largest amplitude and largest frequency (i.e. A_m=1 and f_m =W), then the bandwidth of FM can be simplified as $BW \approx 2(f_\Delta + 2W)$

2. Varactor Diode

Varactor diode is also called tuning diode. Varactor diode is a diode, which its capacitance can be varied by adding a reverse bias voltage to the pn junction. When reverse bias voltage increases, the depletion region becomes wide, this will cause the capacitance value decreases; nevertheless when reverse bias voltage decreases, the depletion region will be reduced, this will cause the capacitance value increases. Varactor diode also can be varied from the amplitude of AC signal. If an AC signal is added to a varactor diode, the variation of capacitance of varactor diode will follow the amplitude of modulating signal.

Figure 5-1 is the analog diagram of capacitance of varactor diode. When a varactor diode without bias, the concentration will be differed from minor carriers at pn junction. Then these carriers will diffuse and become depletion region. The p type depletion region carries electron positive ions, then the n type depletion region carries negative ions. We can use parallel plate capacitor to represent the depletion region.

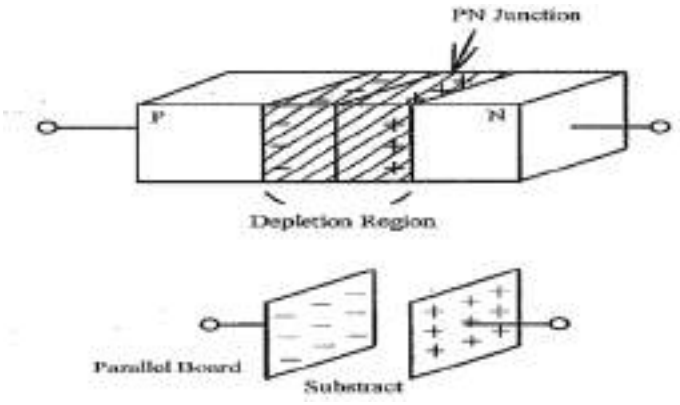

Figure 5-1 The analog diagram of capacitance of varactor diode.

The transition capacitance pn junction of the plates can be expressed as

$$C = \frac{\varepsilon A}{d} \qquad (5\text{-}4)$$

Where

$\varepsilon = 11.8\,\varepsilon_0$, (dielectric constant of Silicon).

$\varepsilon_0 = 8.85 \times 10^{-12}$.

A : The PN junction area. d : Depletion width.

When reverse bias voltage increases, the width of depletion region d will increase but the cross section area A remains, therefore the capacitance value would be reduced. On the other hand, the capacitance value will increase when reverse bias voltage decreases.

Varactor diode can be equivalent to a capacitor series a resistor (Rs) and an inductor (Ls) as

shown in figure 5-2. From figure 5-2, C_j is the junction capacitor of semiconductor, which only exits in pn junction. Rs is the sum of bulk resistor and contact resistor of semiconductor material, which is related to the quality of varactor diode (generally below a few ohm). Ls is the equivalent inductor of bounding wire and semiconductor material.

Tuning ratio, TR is the ratio of capacitance value under two different biases for varactor diode. The expression is shown as follow

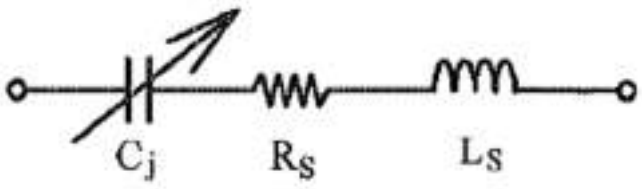

Figure 5-2 The equivalent circuit diagram varactor diode.

$$TR = \frac{C_{V2}}{C_{V1}}$$

Where

TR : Tuning ratio.

Cv_1 : The capacitance value of varactor diode at V1.Cv_2 : The capacitance value of varactor diode at V, .

From this experiment, the characteristics of the varactor diode 1SV55 is shown as below

C_{3V} = 42 pF (The capacitance of varactor diode at bias 3 V). TR= 2.65 (3 V ~ 30 V).

3. Implementation of FM Modulator by Using MC1648 *VCO*

This experiment uses MC1648 VCO to implement the FM modulator, the circuit is shown in figure 5-3. This circuit is an oscillator, which the input terminal of the tuning circuit controls the oscillation frequency. The inputs terminal circuit is a tank circuit as shown in figure 5-4, which includes parallel capacitors and inductors. The capacitors include a ISV55 varactor diode C_d and capacitor C_n lies in between pin IO and pin 12 of MC1648 where C_{in} is approximately 6 pF. If the distributed capacitance is neglected, then the oscillation frequency can be expressed as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \quad - \quad (5\text{-}6) \quad - \frac{1}{2\pi\sqrt{L(C_d+C_{in})}}$$

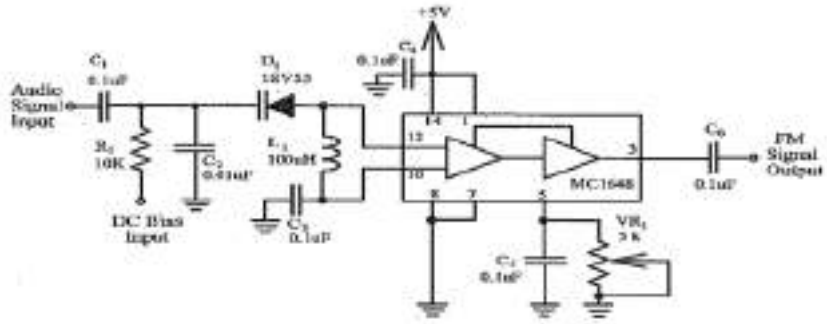

Figure 5-3 The circuit diagram ofMC1648 FM modulator.

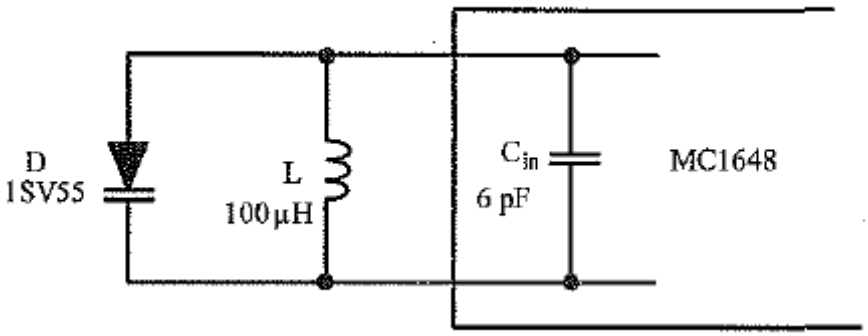

Figure 5-4The tank circuit ofMC1648 FM modulator.

From figure 5-3, C_2 and C_3 are bypass capacitors which are used toremove the noise. The operation frequency of this circuit is approximately 2.4 MHz, and the resistance is approximately only few ohms, therefore, for AC signal, C_2 and C_3 are short circuit, and then C_d and L are parallelto each other. Capacitor C_5 and VR_1 are the charge and discharge loop, which the VR_1 can change the f_0 range. The AC equivalent circuit is shown in Figure 5-4.

When we change the DC bias input terminal, C_d will change andtherefore, the output frequency of oscillator will change too. When the voltage of DC bias input terminal increases (from Figure 5-3, the varactor diode D1 is in reverse bias condition), the C_d decreases and the input frequency of oscillator will increase. On the other hand, when voltage of DC bias input terminal decreases, C_d increases, and the output signal frequency of oscillator will decrease. Therefore, we just need to adjust the DC bias and then add the audio signal to the DC bias, then we can obtain the FM signal from the output terminal of the VCO

4. Implementation of FM Modulator by Using VCO LM566

LM566 is voltage-controlled oscillator integrated circuit. Figure 5-5a is the internal structure diagram of LM566. Figure 5-5b shows the circuit is a main voltage-controlled oscillator LM566 frequency modulator, we let SW_1 open circuit, and the circuit is a voltage-controlled oscillator. The output signal frequency is controlled by C_3, VR_1 and audio signal input terminal voltage. C_2 is used to eliminate parasitic oscillation. If C_3 and VR1 remain a constant, then the output signal frequency and the voltage difference between pin 8 and pin 5 ($V_8 - V_5$) is proportional. In another words, when input signal voltage (V_5) increases, the voltage difference ($V_8 - V_5$) between pin 8 and pin 5 will decrease, the output signal frequency will decrease as well. But, when input signal voltage (V_5) decreases, the frequency of output signal will increase. Another factor that affects the output signal frequency is VR_1 x C_3 value, the output signal frequency and VR_1 x C_3 is inverse proportionally. When the VR_1 x C_3 value is getting larger, the output signal frequency is getting lower. But when the VR_1 x C_3 value is getting smaller then the output signal frequency is getting higher. From figure 5-5, when we short circuit SW_1, then R_1 and R_2 provide a DC bias voltage as the DC level of input audio signal. The center frequency (f_0) can be adjusted by using VR_1. If audio signal input terminal is inputted with an AC signal, the VCO output signal frequency will follow the change of the input audio signal voltage, which the FM signal is deviated.

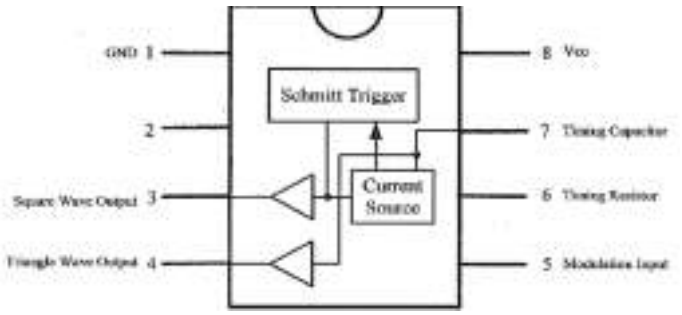

Figure 5-5aThe internal structure diagram ofLM566.

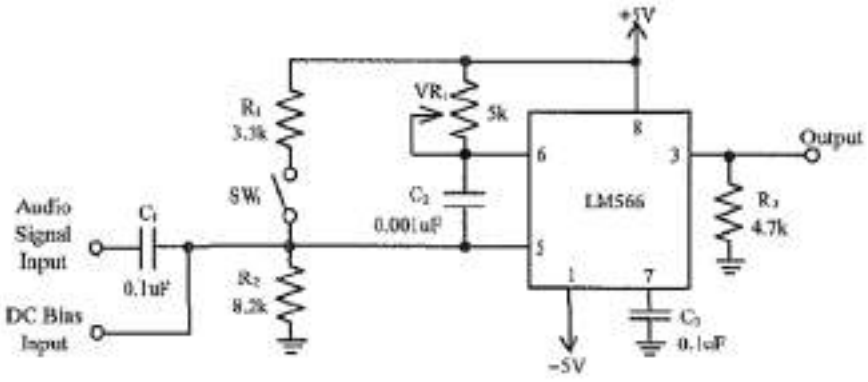

Figure 5-5b The circuit diagram of LM566 FM modulator.

Experiment Items

Experiment 1: The basic characteristic measurement ofMC1648 voltage controlled oscillator

1. Refer to figure 5-3 or ETEK DA-2000-03 module, let J1 be open circuit, so that the D_1 bias will operate from forward bias input to the terminal I/P2 input, at the same time let J3 be short circuit and J2 be open circuit, that means L_1 =100 µH.

2. From forward bias input to the terminal I/P2, input 3V of forward voltage, by using oscilloscope, observe on the output signal waveform; adjust VR_1 until output signal is sine wave frequency, records the output signal frequency in table 5-1.

3. Refer to table 5-1 voltage conversion input forward bias, by using oscilloscope, observe on the output signal waveform, then record the output signal frequency in table 5-1.

4. From table 5-1, gets the data and plots the characteristic curve of frequency versus voltage.

Experiment 2: MC1648 frequency modulator

1. Refer to figure 5-3 or ETEK DA-2000-03 module. Let J1 be short circuit,so that D_1 bias operates at 5 V, at the same time let J3 be short circuit andJ2 be open circuit, and now let Inductor L_1 is 100 µH. Now, we call the output signal frequency as cutoff frequency f_C

2. From the audio signal input port (I/ Pl), input 2 VPP amplitude and 3 kHz sine wave frequency. Adjust VR_1 so that output signal is sine wave.

3. By using spectrum analyzer, observe on the frequency spectrum of output signal and record the measured results in table 5-2.

4. Change the audio signal frequencies to 5 kHz and 8 kHz; the others remain the same. Repeat step 3.

   Note: There is a big difference between carrier frequency and modulated signal frequency, if using oscilloscope to observe the time and the change is not clear, we can use spectrum analyzer to observe FM frequency spectrum.

Experiment 3: The basic characteristics measurement ofLM566VCO

1. Refer to figure 5-5 or ETEK DA-2000-03 module, let J1 be open circuit.The circuit now is voltage controlled oscillator. Let J2 be short circuit,J3 be open circuit, that means C_3 is 0.1 µF.

2. From the forward voltage input port (pin 5), input 3.6 V forward voltage, then adjust VR_1 so that output signal frequency is 2 kHz. Now, we call this frequency as cut off frequency f_C.

3. Adjust forward voltage input port (pin 5) so that the input signals are 2.7 V, 3.0 V, 3.3 V, 3.9 V, 4.2 V and 4.5 V. By using oscilloscope, observe on the output signal waveform and record the output signal frequency in table 5-3.

4. Plot the characteristic curve of frequency versus voltage in figure 5-7.

5. Let J3 be short circuit, J2 be open circuit, and now change C_3 to C_4, which is 0.1 µF to 0.01 µF.

6. From the forward bias input port (pin 5), input 3.6 V forward voltage, then adjust VR_1 so that the output signal frequency is 20 kHz. Now, we call this frequency as cutoff frequency f_C.

7. Adjust forward voltage input port (pin 5) so that the input signals are 2.7 V, 3.0 V, 3.3 V, 3.9 V, 4.2 V and 4.5 V. By using oscilloscope, observe on the output signal waveform and record the output signal frequency intable 5-4.

8. Plot the characteristic curve of frequency versus voltage in figure 5-8.

Experiment 4: LM566 VCO frequency modulator

1. From figure 5-5 or ETEK DA-2000-03 module, let JI be short circuit, at this moment this circuit is frequency modulator, then let J3 short circuit, J2 be open circuit, and now the capacitor C_4 is 0.01 µF. Adjust VR_1 until the output signal frequency is 20 kHz.

2. From the audio signal frequency input port (I/P), input 1.6 V_{pp} amplitude and 1 kHz sine wave frequency. By using oscilloscope, observe on the output signal waveform and record the measured results in table 5-5.

3. Change the audio signal frequencies to 3 kHz and 5 kHz, the others remain the same. Observe on the output signal waveform and record the measured results in table 5-5.

4. From the adjust audio signal input port (I/P), input 2 V_{pp} amplitude signal and 1 kHz sine wave frequency. By using oscilloscope, observe on the output signal waveform and record the measured results m table 5-6.

5. Change audio signal frequencies to 3 kHz and 5 kHz, the others remain the same. By using oscilloscope, observe on the output signal waveform and record the measured results in table 5-6.

Measured Results

Table 5-1 The measured results of MC1648 voltage controlled oscillator.

Input Forwardbias (V)	3	4	5	6	7	8	9	10	11	12	13	14
Frequencies(MHz)	3	4	5	6	7	8	9	10	11	12	13	14

Output Signal Frequency (MHz)

3 4 5 6 7 8 9 10 11 12 13 14

Table 5-2 The measured results of MC1648 frequency modulator (V_m = 2 V_{pp}).

Input Signal Frequencies	Input Signal Waveforms .	Output Spectrum frequencies
3kHz		
5kHz		
8kHz		

Table 5-3 The measured results of LM566 voltage controlled oscillator ($C_3 = 0.1\mu F, f_0$ =2kHz).

Input Voltage Conversion (V)	2.7	3.0	3.3	3.6	3.9	4.2	4.5
Input Signal Frequencies (Hz)							

Output Signal Frequency (MHz)

3 4 5 6 7 8 9 10 11 12 13 14

Table 5-4 The measured results of LM566 voltage controlled oscillator ($C_4 = 0.01\,\mu F$, $f_0 = 20\,kHz$).

Input Voltage Conversion (V)	2.7	3.0	3.3	3.6	3.9	4.2	4.5
Output Signal Frequencies (Hz)							

Output Signa **Frequency** (MHz)

3 4 5 6 7 8 9 10 11 12 13 14

Table 5-5 The measured results of LM566 frequency modulator (V_m = 1.6 VPP , C_3 = 0.01 µF, f_0 = 20 kHz).

Input Signal Frequencies	Input Signal Waveforms	Output Signal Waveforms
1 kHz		
3 kHz		
5 kHz		

Table 5-6 The measured results of LM566 frequency modulator (V_m = 2 VPP , C_3 =0.0lµF, f_0 =20kHz).

Input Signal Frequencies	Input Signal Waveforms	Output Signal Waveforms
1 kHz		
3kHz		

5kHz		

Problems Discussion

1. Refer to figure 5-3 MC1648 frequency modulator, if using 80 nH inductor, what is the required capacitance of the varactor diode in order to oscillate at 100 MHz for the tank circuit?

2. From the characteristic curve in table 5-1, which part of the curve is the most suitable for designing the frequency modulator? Why?

3. From figure 5-5 frequency modulator, when Jl short circuit, what are the objectives of R_1 and R_2?

FM DEMODULATION

Curriculum Objectives

1. To understand the operation theory of phase locked loop.
2. To understand the basic characteristics of LM565 phaselocked loop.
3. To design and implement the phase locked loop to demodulate the modulated signal.
4. To design and implement the frequency discriminator todemodulate the modulated signal.

Curriculum Theory

Frequency demodulator is also called frequency discriminator, which can convert the variation of frequency to the variation of linear voltage. Normally we use FM to AM conversion circuit, balanced discriminator circuit, phase-shift discriminator circuit and PLL synthesizer for the FM demodulator. In this chapter, we will introduce the phase locked loop frequency demodulator and FM to AM conversion discriminator.

1. The Operation Theory of Phase Locked Loop

Phase locked loop or PLL is a feedback circuit. In the feedback loop, the feedback signal will lock the output signal frequency and phase with the same frequency and phase of the input signal. So, for wireless communication, if the frequency of the carrier signal deviation during transmission, then the PLL in the receiver will operate and lock the carrier signal. In this

experiment, there are two types of using PLL, and the first type is demodulator, which is used for demodulation by following the variation of phase and frequency. The second is the carrier frequency tracking which is used to track the changes of the frequency of the carrier signal and synchronize the oscillation.

Normally, phase locked loop can be divided into 3 sections, there are

1. Phase detector (PD)
2. Low-pass filter (LPF)
3. Voltage controlled oscillator (VCO)

From figure 6-1, the function of phase detector is to receive input signal and VCO signal, then the two signals are compared by phase detector and provided an output signal, which is a pulse signal. After that this signal is then sent to a low-pass filter to remove the unwanted signal and left the DC voltage.

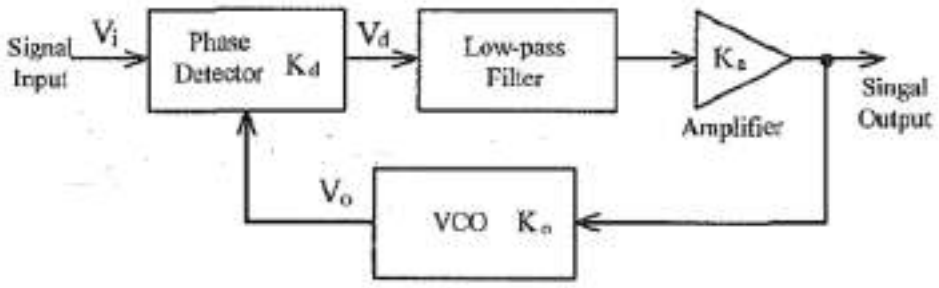

Figure 6-1 The block diagram of phase locked loop.

This DC voltage can be used to control the output signal frequency of VCO. Figure 6-1. is the block diagram of phase-locked loop, where

K_d = The gain of phase detector (Volts/Radian)

Ka = The gain of amplifier (Volt/Volt)

K_0 =The gain of VCO (kHz/Volt)

$K_L = K_d K_a K_o$= The gain of closed loop (kHz/Radian)

We use a simple circuit to explain the basic concept of phase detector. From figure 6-2(a) shows the phase difference between two input signals is the smallest, so the output signal pulse width is the narrowest. Then figure 6-2(b) shows the phase difference between two input signals is larger than figure 6-2(a), so the output signal pulse width is wider than figure 6-2(a). Figure 6-2(c) shows the phase difference between two input signals is the largest and therefore the output signal pulse width is the widest.

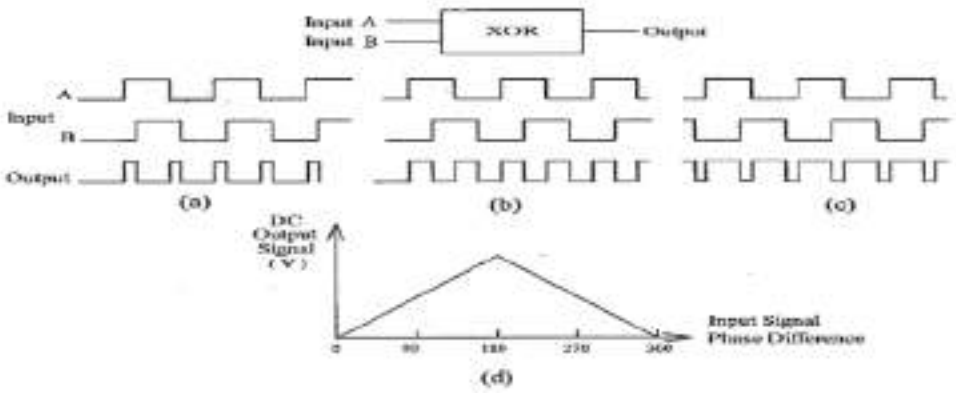

Figure 6-2 The theory of phase detector.

If this three output signals pass through the low-pass filter to remove the AC signal, then the magnitude of DC voltage in figure 6-2 is as follow: 1. figure 6-2(c) has the highest DC voltage, 2. figure 6-2(b) is the second higher, and 3. figure 6-2(a) is the lowest. The relation of DC voltage and the phase difference of A, B input signals is shown in figure 6-2(d).

From figure 6-3, assume that the free-running frequency of a VCO is set to 1 kHz (assume the bias voltage is 2 V). If inputting a signal A is below 1 kHz and a signal B is higher than 1 kHz. From figure 6-3, we found that, when input signal A frequency lower than the free-running frequency of VCO, then the output of low-pass filter will receive a lower voltage level (assume is I V), this lower voltage level will adjust the oscillation frequency of VCO, so that the oscillation frequency will decrease until the frequency of output signal of VCO and the frequency of signal A equal to each other. When input signal B frequency is higher than the basic frequency of VCO, the output terminal of low-pass filter will receive a higher voltage (assume is 3 V), so that the oscillation frequency of VCO will increase until the frequency of output signal of VCO and the frequency of signal B equal to each other. Normally the time needed for VCO locked frequency is very short. Above is just an ideal explanation. In fact the phase detector circuit is not as easy as you think.

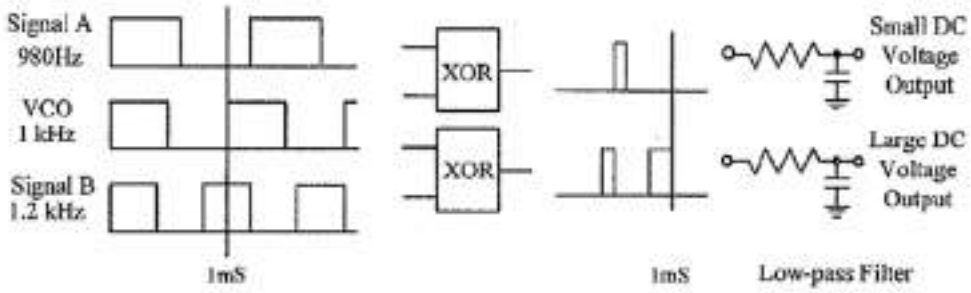

Figure 6-3 The theory of locked frequency.

1. The Basic Characteristics of **LM565 PLL** Circuit

(I) Free-running frequency Figure 6-4 is a LM565 phase locked loop circuit diagram, from figure when input terminal does not input any signal, the output signal frequency of VCO is called free-running frequency. Where C2 is timing capacitor, VR_1 is timing variable resistor, the free-running

frequency (f_0) of LM565 is decided by C_2 and VR1.

Free-running frequency: $f = \frac{f_0 1}{3.7VRI\ c}$ (6-1)

Closed loop gain: $K_L = K_d K_a K_o = \frac{33.6 f_o}{V_c}$ (6-2)

Where V_c= Total voltage supply= V_{cc} -(-V_{cc})= 5-(-5) =10 V

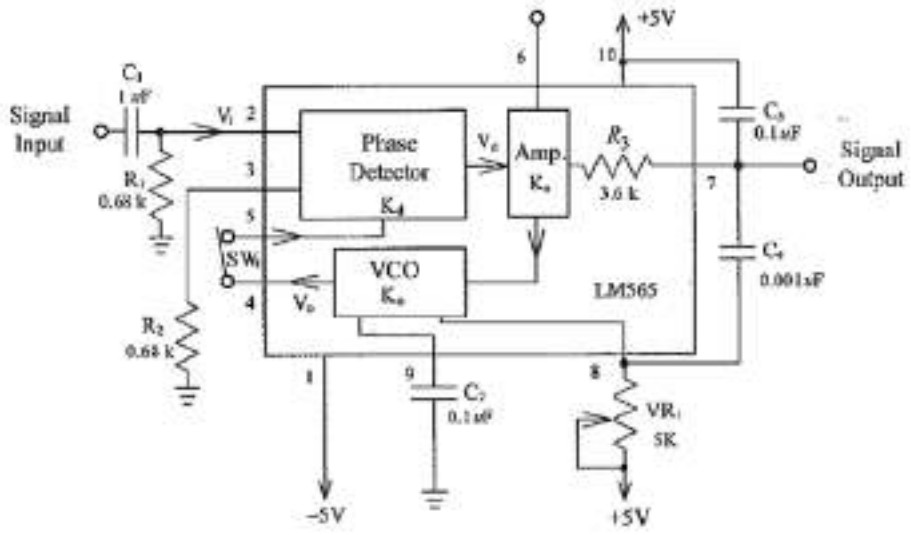

Figure 6-4 LM565 phase locked loop.

1. Locked Range

When phase-locked loop circuit is at already-locked situation, assumethe input signal frequency (f_i) slowly move away from f_0, when f_i reaches at a certain frequency, the PLL will

leave the locked situation. At this moment, the maximum frequency difference for frequency f_i and f_0 is called locked-range (refer to figure 6-5). The locked-range of LM565 is

$$f_L = \frac{8 f_o}{V_c} \qquad (6\text{-}3)$$

2. Captured Range

At the beginning, PLL is at not locked situation, and then let the input signal frequency f_i slowly move close to f_o, when f_i reaches at a certain frequency, PLL will be at already-locked situation. Then at this moment, the frequency difference between f_i and f_0 is called captured range (refer to Figure 6-5). LM565 captured range is

$$f_c = \left(\frac{1}{2\pi}\right)\sqrt{\frac{2\pi f_L}{3.6\times10^3\times C_2}}$$

(6-4)

3. Implementation of FM demodulator by Using LM565 **PLL**

Figure 6-4 is the circuit diagram of LM565 phase-locked loop, we can use this circuit as a FM demodulator. When the input signal frequency increases, then the output signal voltage decrease. However, when the input signal frequency decreases, the output signal voltage will increase, therefore, we can utilize the relationship between the voltage of PLL and frequency to design the FM demodulator. LM565 phase detector and VCO are designed in the IC package, this VCO and LM566 are the same. The free-running frequency f0 of VCO is decided by the external C_2 and VR_1. The low-pass filter is comprised by the internal resistor R_3 at pin 7 and external capacitor C_3. The objective of capacitor C_4, which is connected between pins 7 and 8 is to reduce the parasitic oscillation.

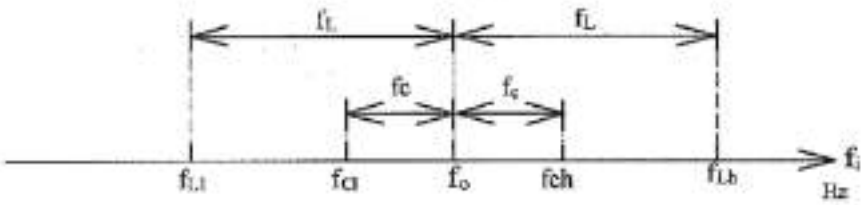

Figure 6-5 Lock range and capture range diagram.

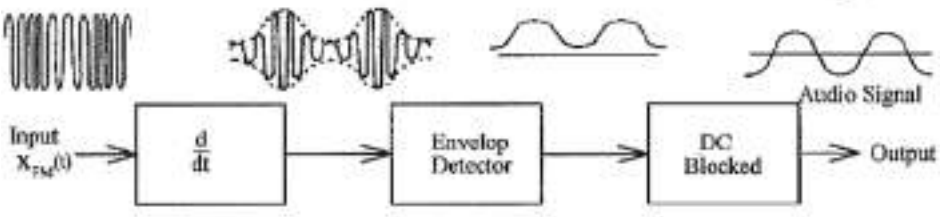

Figure 6-6 The block diagram of FM to AM frequency discriminator.

2. FM to AM Conversion Discriminator

Figure 6-6 is the block diagram of FM to AM frequency discriminator, which is used to convert the FM signal through a differentiator to AM signal, then use an AM envelope detector to demodulate.

From figure 6-6, the input signal $X_{FM}(t)$ is

$$x_{FM}(t) = A_c \cos\theta(t) = A_c \cos\left[2\pi f_c t - 2\pi f_\Delta \int x(\lambda)\, d\lambda\right] \qquad (6\text{-}5)$$

After passing through a differentiator, the output signal is

$$x'_m(t) = -A_C\theta'(t)\sin\theta(t)$$

$$= 2\pi A_C[f_C + f_\Delta x(t)]\sin[\theta(t)+180°] \qquad (6\text{-}6)$$

From equation (6-6), we know that $x'_{FM}(t)$ amplitude is varied from x(t). Therefore, this signal is an amplitude modulation signal, and when this signal is sent to an envelope detector, then we can obtain the demodulated audio signal. The actual circuit diagram is shown in figure 6-7.

From figure 6-7, U_1.C_1.C_2,R_1 and R_2 comprise a differentiator, U_2,R_3 and R_4 comprise an inverting amplifier, D_1, R_5,R_6.C_4 and *Cs* comprise AM peak detector. Capacitor C_6 is used to block the DC voltage signal. Due to U_1 and U_2 need the operation frequency at near 1.5 MHz, so µA741 is not suitable to use in this case, therefore, we choose LM3l 8, which provides better frequency response.

Besides the above mentioned FM demodulator, there is another band pass filter constructed by

LC circuit also frequently be used in FM demodulator at high frequency and microwave frequency. Figure 6-8 is the frequency response of band pass filter. The frequency response of band pass filter curve depends on the voltage level and also varied from the frequency, therefore, we can apply this characteristic on the discriminator.

Experiment Items

Experiment 1: The basic characteristics measurement ofLM565 phase locked loop

1. Refer to figure 6-4 or ETEK DA-2000-03 module. Let J2 be short circuit and J3 be open circuit, then C_2 is 0.1 μF.

2. Let JI be open circuit, which let SW_1 be open circuit.

3. Adjust the variable resistor VR_1, then measure the output signal of LM565 VCO at pin 4 under the largest free-running frequency f_{0h} and the smallest free-running frequency f_{o1} (refer to figure 6-5) and record the measured results in table 6-1.

4. Adjust the variable resistor VR_1 until the free-running frequency of VCO output (f_O) is 2 kHz.

5. Let JI be short circuit, and from the input port, input 0.25 V_{pp} amplitude and 2 kHz square wave frequency.
6. By using oscilloscope, observe on the input signal and output signal of LM565 VCO (pin 4). Slightly adjust the input signal frequency, when VCO output signal frequency stable and cannot lock input signal, record the signal frequency f_{Lh} at this moment in table 6-1.
7. Readjust the input signal frequency to the free-running frequency (f0) of VCO. Then decrease the input signal frequency, when output signalfrequency of VCO cannot lock the input signal, record the input signalfrequency f_{L1} at this moment in table 6-1.

8. By using equation $f_L = (f_{Lh} - f_{L1})/2$, then calculate the locked range.

9. Increase the input signal frequency, so that the output signal frequency of VCO cannot lock the input signal. Then slightly decrease the input signal frequency until the phase locked loop locks the input signal. observe on the input signal frequency f_{ch} and record the measured results in table 6-1.

10. Decrease the input signal frequency so that the output signal frequency of VGO-cannot-lock the input signal. Then slightly increase the input signal frequency until the phase locked loop locks the input signal. Observe on the input signal frequency fc1 and record the measured results in table 6-1.

11. By using equation $fc = (f_{ch} - f_{c1}) / 2$, then calculate the captured range.

12. Let JI and J2 be open circuit, J3 be short circuit, which means that C_2 changes to C_5, i.e. 0.1 µF changes to 0.01 µF, then repeat step 3.

13. Adjust the variable resistor VR_1, so that the free-running frequency (f_0) of the VCO output signal is 20 kHz. Let JI be short circuit and from theinput terminal, input 0.25 V_{pp} amplitude and 20 kHz square wavefrequency, then repeat step 6 to step 11.

Experiment2: The characteristics of voltage and frequency conversion ofLM565 PLL

I. Refer to figure 6-4 and connect the circuit or refer to ETEK DA-2000-03 module. Let J2 be short circuit and J3 be open circuit, i.e. C_2 is 0.l μF.

2. Let JI be open circuit, adjust the variable resistor VR_1 so that the free-running frequency (f_o) of the output signal of VCO LM565 at pin 4 is 2 kHz.

3. Let JI be short circuit, which means SW_1 short circuit.

4. From the signal input terminal, input 0.5 V_{pp} amplitude and 2 kHz square wave frequency, then measure the voltage of output terminal (LM565 pin 7) and record the measured results in table 6-2.

5. Change the input signals to 0.5 kHz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3 kHz and 3.5 kHz, respectively. Then measure the voltage of output terminal and record the measured results in table 6-2.

6. Plot the characteristic curve of voltage versus frequency in figure 6-9.

7. Let J3 be short circuit and J2 be open circuit, which means that C_2 changes to C_5, i.e. 0.1 μF changes to 0.01 μF.

8. Let JI be open circuit, adjust the variable resistor VR_1 so that the free-running frequency (f_0) of the output signal of VCO LM565 at pin 4 is 20 kHz.

9. Let J1 be short circuit, which means SW_1 be short circuit .

10. From the signal input terminal, input 0.5 V_{pp} amplitude and 20 kHz square wave frequency, then measure the voltage of output terminal (LM565 pin 7) and then record the measured results in table 6-3.

11. Change the input signals to 6.5 kHz, 17.5 kHz, 18.5 kHz, 20 kHz,

21.5 kHz, 22.5 kHz and 23.5 kHz, respectively. Then measure the voltage of output terminal and record the measured results in table 6-3.

12. Plot the characteristic curve of voltage versus frequency in figure 6-10.

Experiment 3: Phase locked loop frequency demodulator

1. Refer to figure 5-5 in chapter 5 or ETEK DA-2000-03 module, let Jl be short circuit. Next let J3 be short circuit and J2 be open circuit, which means C_4 is 0.01 μF. Adjust VR_1 so that the free-running frequency (f_o) of the output signal is 20 kHz.

2. Refer to figure 6-4 or ETEK DA-2000-03 module, let J3 be short circuit, Jl and J2 be open circuit, which means C_5 is 0.01 μF, then adjust the free-running frequency (f_o) of the VCO output to 20 kHz.

3. Let output terminal of LM566 VCO frequency modulator connects to the input terminal of LM565 PLL frequency demodulator. Next let Jl be short circuit.

4. Adjust the function generator to output 600 mV_{pp} amplitude and 1 kHz positive square wave frequency, then input this signal to the input terminal of LM566 VCO frequency modulator (refer to figure 5-5). By using oscilloscope, observe on the output signal waveform of LM565 PLL frequency demodulator and record the measured results in table 6-4.

5. Change the input signal frequencies to 800 Hz and 1.2 kHz, repeat step

6. Adjust the amplitude of the signal to 300 mV_{pp}; the others remain the same. Repeat step 4, then record the measured results in table 6-5.

7. Change the input amplitude of the signal to 600 mV_{pp} and 800 mV_{pp}, repeat step 4, then record the measured results in table 6-5.

Experiment4: FM to AM conversion frequency demodulator

1. Refer to figure 5-3 in chapter 5 or ETEK DA-2000-03 module, let J1 be short circuit, which means the operation bias voltage of varactor diode D_1 is 5 V. Then let J2 be open circuit and J3 be short circuit, i.e. L_1 is 100 μH.

2. From the input terminal (I/Pl) of the audio signal of MC1648 frequency modulator in figure 5-3, input 2 V_{pp} amplitude and 1 kHz square wave frequency, then adjust VR_1 so that the output signal amplitude is maximum.

3. Refer to figure 6-7 or ETEK DA-2000-03 module, connects the output terminal of MC1648 frequency modulator in figure 5-3 to the input terminal of frequency modulation signal.

4. By using oscilloscope, observe on the input signal waveform of frequency modulation and the output signal waveform of frequencydemodulator, then record the measured results in table 6-6.

5. Change the audio signal in step 2 to 2 kHz and 3 kHz, repeat step 4.

Measured Results

Table 6-1 The measured results of the basic characteristics of LM565 PLL.

C_2	f_o	Free-running Frequency Range		Locked Range f_L		Captured Range f_c	
		f_{oh} .	f_{ol}	f_{Lh}	f_{L1}	f_{ch}	f_{c1}
0.1 µF	2 kHz	Hz	Hz	Hz	Hz	Hz	Hz
				f_L= Hz		f_c= Hz	
0.01 µF	20 kHz	Hz	Hz	Hz	Hz	Hz	Hz
				f_L= Hz		f_c= Hz	

Table 6-2 The measured results of the voltage and frequency conversioncharacteristics ofLM565 PLL (Vm=0.5 V_{pp}, f_o=2 kHz, C_2=0.1 µF).

Input Signal Frequencies(kHz)	0.5	1.0	1.5	2.0	2.5	3.0	3.5
Output Voltages (V)							

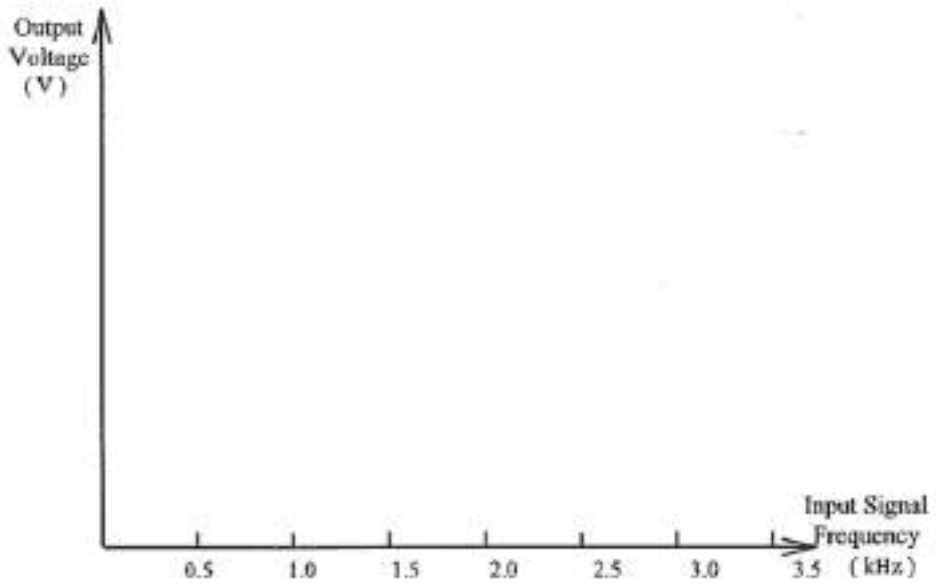

Figure 6-9 The characteristics curve of voltage versus frequency.

Table 6-3 The measured results of the voltage and frequency conversioncharacteristics of LM565 PLL (V_m = 0.5 V_{pp}, f_o =20 kHz, C_5 = 0.0I µF).

Input Signal Frequencies (kHz)	. 16.5	17.5	18.5	20	21.5	22.5	23.5
Output Voltages (V)							

Figure 6-10 The characteristic curve of voltage versus frequency.

Table 6-4 The measured results of the input and output signal waveforms of PLL frequency demodulator (Vm = 600 mV_{PP}, f_o = 20 kHz).

Audio Signal Frequencies	Input Signal Waveforms	Output Signal Waveforms
1 kHz		
800Hz		
1.2 kHz		

Table 6-5 The measured results of the input and output signal waveforms of PLL frequency demodulator (f_m=1 kHz , f_o = 20 kHz).

Audio Signal Amplitude	FMI/P	Audio O/P
300mV_{pp}		
600 mV_{pp}		-
800 mV_{pp}		

Table 6-6 The measured results of the input and output signal waveforms of FM to AM conversion frequency demodulator (Vm=2Vpp)

Audio Signal Frequencies	Frequency DemodulatorInput Signal Waveforms	Frequency Demodulator Output Signal Waveforms
1 kHz		
2kHz		
3 kHz		

Problems Discussion

1. From the measured results of the basic characteristics experiment of LM565 PLL, when the input signal frequency moves away from the frequency locked range, what is the oscillation frequency of the VCO?

2. For LM565 PLL, compare the locked range and the captured range.

3. In figure 6-4, what are the functions for capacitor C_3? If let C_3 change from 0.1 μF to 0.01 μF, what are the changes of the pin 7 ofLM565?

4. In the LM565 frequency demodulator experiment, if the output signal passes through the first order low-pass filter, then is the output signal flatter than the previous one? Try to design the low-pass filter.

5. How to use the PLL circuit and the logic circuit to comprise a double frequencies circuit?